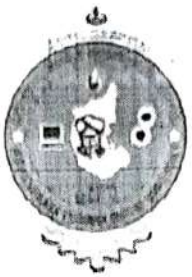
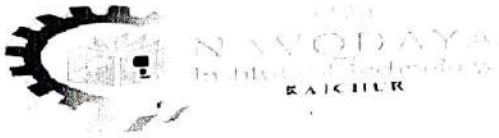
Civil Engineering

VISVESVARAYA TECHNOLOGICAL UNIVERSITY,
JNANA SANGAMA, BELAGAVI - 590 018



NET'S
NAVODAYA INSTITUTE OF TECHNOLOGY
RAICHUR - 584103



A

PROJECT REPORT

ON

"A STUDY ON ASSESSMENT OF BLACK COTTON SOIL AS A RAW MATERIAL FOR MANUFACTURING BRICKS BY USING FLY ASH AS A STABILIZER."

Submitted By

MOHAMMED MANSOOR	(3NA12CV011)
SHAIK NASEERUDDIN PATEL	(3NA12CV021)
TOUSIF SHABBIR GHETA	(3NA12CV025)
MOHAMMED ZUBER	(3NA13CV420)

Under The Guidance Of

Prof. RAJMOHAN B

DEPARTMENT OF CIVIL ENGINEERING

2015-2016

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

2020/9/18 18.32

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, JNANA SANGAMA, BELAGAVI- 590 018

NET'S

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR - 584103

DEPARTMENT OF CIVIL ENGINEERING

CERTIFICATE

This is to certify that **Mr. MOHAMMED MANSOOR** *(3NA12CV011),* **SHAIK NASEERUDDIN PATEL** *(3NA12CV021),* **TOUSIF SHABBIR GHETA** *(3NA12CV025),* **MOHAMMED ZUBER** *(3NA13CV420) of B.E. 8th Semester has successfully completed the project work entitled* **"A STUDY ON ASSESSMENT OF BLACK COTTON SOIL AS A RAW MATERIAL FOR MANUFACTURING BRICKS BY USING FLYASH AS A STABILIZER"** *for the partial fulfillment of Bachelor of Engineering in* **CIVIL ENGINEERING** *as prescribed by the Visvesvaraya Technological University, Belagavi, during the academic year 2015-16.*

Project Guide	***Head of the Department***	***Principal***
Prof. RAJMOHAN B	***Dr. SHIVAREDDY M. S***	***Dr. SHIVA PRAKASH C.K***

Name of Examiners:

1. 1016

2.

Signature with date

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

2020/9/18 18:33

DECLARATION

We hereby declare that, the Project Report entitled, "A STUDY ON ASSESSMENT OF BLACK COTTON SOIL AS A RAW MATERIAL FOR MANUFACTURING BRICKS BY USING FLYASH AS A STABILIZER", which is submitted here with for the award of degree of Bachelor of Engineering in CIVIL ENGINEERING of Visvesvaraya Technological University, Belgaum during the year **2015-16** is the result of the work done by us at Department of CIVIL ENGINEERING a **NAVODAYA INSTITUTE OF TECHNOLOGY, RAICHUR.** Under the guidance of [redacted]. We further declare that, the matter embodied in this project work have not been previously submitted by me for award of any other degree.

Date:

Place: Raichur

MOHAMMED MANSOOR **(3NA12CV011)**

SHAIK NASEERUDDIN PATEL **(3NA12CV021)**

TOUSIF SHABBIR GHETA **(3NA12CV025)**

MOHAMMED ZUBER **(3NA13CV420)**

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

2020/9/18 18:33

ABSTRACT

Black cotton soil is one of the major soil deposits in India covering approximately about 16% of the total land area of the country: so, it is a very good opportunity to use black cotton soil as a raw material for manufacturing burnt clay bricks. But, due to its high potential to swell and shrink it is not possible to use it in manufacturing burnt clay bricks. From the past research it is found that the swelling and shrinkage property of black cotton soil can be improved by the addition of fly ash to it. At the same time large quantity of fly ash is being generated from huge number of thermal power plants and readily available for the usage. Thus, this work was oriented towards using black cotton soil and fly ash in combination for manufacturing of burnt clay bricks.

In this experimental investigation an effort has been made to study the feasibility of producing bricks from locally available black cotton soil (also called black soil) using industrial waste materials such as fly ash as a stabilizer. In this study the various engineering properties of bricks such as compressive strength, water absorption test and efflorescence test were assessed. For this purpose, a total of 54 numbers of brick specimens of 210x100x75mm size were prepared in series by combining black soil and fly ash in six different proportions. Thus prepared specimens were then air dried, baked in kiln and tested for engineering properties as per IS 3495 code procedure.

Also for comparison purpose, 9 numbers of conventional burnt clay bricks, 9 numbers of red earth burnt clay bricks and 9 numbers of pressed type water cured cement fly ash bricks were tested for the aforesaid engineering properties. Test results obtained in the present investigation indicated that it is possible to manufacture good quality bricks by using locally available black soil by suitably adding fly ash and such bricks can be used in lieu of conventional burnt clay bricks or pressed type water cured cement fly ash bricks presently in use for various construction activities across the country.

Key Words: Black cotton soil, Fly ash, Compressive strength, Efflorescence, Water absorption.

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

2020/9/18 18:33

CONTENTS

Chapter 4: MANUFACTURING OF BRICKS

Chapter 1: INTRODUCTION

1.1 Black Cotton Soil

Black soil is one of the major soil deposits in India covering an area of about 5.4 lakh square kilometer i.e. 16.6% of the total land area of our country at present, Black soils, locally called as black cotton soils and internationally known as 'tropical black earths' or 'tropical chernozems' have been developed by the weathering of the Deccan lava in major parts of Maharashtra, western Madhya Pradesh (Hoshangabad, Narsinghpur, Damoh, Jabalpur, Raisen and Shahdol districts), Gujarat (Surat, Bharuch, Vadodara, Kheda, Sabarkantha and Dang districts), Andhra Pradesh (Adilabad, Warangal, Khammam, Mahbubnagar, Kurnool, Guntur and Karimnagar districts), Karnataka (Bijapur, Dharwar, Gulbarga, Bidar, Belgaum, Raichur, Bellari and Chitradurga districts), Rajasthan (Kota, Bundi, SawaiMadhopur, Bharatpur and Banswara districts), Tamil Nadu (Ramnathpuram, Tirunelvelli, Coimbatore, Madurai and South Arcot districts) and Uttar Pradesh (Jalaun, Hamirpur, Banda and Jhansi districts).

There are no large-scale brick manufacturing kilns available to cater to the needs of various construction activities. This increases the cost of bricks which in turn increases the overall cost of projects in these regions by about 15 to 20%. Generally quality of bricks mainly depends on the type and quality of raw materials used for manufacturing them. It is a well-established fact that good quality bricks can be manufactured from alluvial/red soil.

Black cotton soil is a highly clayey soil and the black colour in black cotton soil is due to the presence of titanium oxide in small concentration. The black cotton soil has a high percentage of clay, which is predominantly montmorillonite in structure and black or blackish grey in colour. Expansive soils are the soils which expand when the moisture content of the soil increases. The clay mineral montmorillonite is mainly responsible for expansive characteristics of the soil.

1.2 Problems Associated With Usage of Black Cotton Soil In Brick Manufacture Industry

- BCS exhibits high swelling/shrinkage propensity due to the presence of mineral montmorollonite.
- It is very difficult to handle/mix BCS due to its high plasticity.
- Though the bricks are casted with BCS, they develop severe cracks after drying/burning due to their higher shrinkage propensity.
- Also, the compressive strength of BCS is very less when compared to other type of bricks.

1.3 Possible Solutions For Overcoming Above Problems

It is necessary to do something to BCS to make use of it in the manufacturing of bricks. Following are some of the possible solutions to overcome the problems associated with BCS.

- An industrial waste such as fly ash can be utilized for stabilizing/improving the engineering properties of BCS.
- The addition of FA to BCS can reduce shrinkage, water absorption and swelling propensity of black cotton soil.
- A proper/standard method of production of bricks has to be adopted for manufacturing of bricks.

3.2 Experimental Program

3.2.1 Mix Proportions

Sl.no	MIX	Proportion
1	M1	100% BCS + 10%FA
2	M2	90% BCS + 10% FA
3	M3	80% BCS + 20% FA
4	M4	70% BCS + 30% FA
5	M5	60% BCS + 40% FA
6	M6	50% BCS + 50% FA

Table 4: Mix proportions

3.2.2 Tests on various soil – Fly ash mix proportions

a. Liqud limit test
b. Plastic limit test
c. Plasticity index
d. Free swell test

a. LIQUID LIMIT:

Liquid limit (LL or *wL*) is defined as the arbitrary limit of water content at which the soil is just about to pass from the plastic state into the liquid state. At this limit, the soil possesses a small value of shear strength, losing its ability to flow as a liquid. In other words, the liquid limit is the minimum moisture content at which the soil tends to flow as a liquid

3.2.4 Discussion on results of tests

a. **Liquid limit**

It was observed that there was sudden decrease in liquid for 10% and with a slight reduction upto 30% fly ash content, then started gradually reducing till 50% fly ash content. Hence it can be suggested that liquid limit decreases with increase in fly ash content

b. **Plastic limit**

From the results of plastic limit it was found that plastic limit was maximum for 0 – 10 % fly ash content, then there was sudden decrease upto 30% of fly ash content and further remained constant for 40% with gradual decrease in value till 50% of fly ash content. Hence it was concluded that the plastic limit decreases with increase in fly ash content

c. **Plasticity index**

From plasticity index we came to know that there was slight increase in plasticity index till 30% of fly ash content and there was drastically decrease in plasticity index upto 50% of fly ash content

d. **Free swell**

It was observed that there was sudden decrease in swelling upto 20% of fly ash content, decreases gradually till 50% of fly ash content. Hence addition of fly ash decreases swelling potential of black cotton soil

Chapter 7: CONCLUSION

Based on the test carried out and observed results, following conclusions can be drawn.

1. It is not possible to manufacture brick by using black cotton soil only due to its high plasticity and high propensity to shrink and swell.
2. The bricks manufactured by using only BCS developed severe cracks during drying and burning.
3. It is found that the FA content is not having any definite effect on plasticity index of BCS however the addition of fly ash to BCS will ease the handling of mix.
4. The addition of fly ash to BCS will reduce the swelling potential of BCS higher the content of fly ash, lower will be the swelling potential.
5. It is possible to manufacture bricks using BCS as a raw material and fly ash as stabilizer.
6. The maximum compressive strength can be achieved by the addition of 30% of fly ash by weight to BCS, however the compressive strength of bricks was degrading beyond 30% of fly ash.
7. The compressive strength obtained for brick with mix M2, M3 and M4 were higher than conventionally used red earth bricks.
8. The minimum water absorption was found in mix M2, however, the water absorption for all mixer are within the limits, thus water absorption is not a problem with BCS-fly ash brick.
9. When compared all other conventional type of bricks the water absorption levels are very less in BCS – fly ash bricks.
10. No efflorescence was found in any of the BCS – fly ash bricks it may be due to absence of salts in BCS – fly ash bricks.
11. If BCS and fly ash are readily available in particular locality, then BCS –fly ash bricks can be manufactured at very low cost.
12. The utilization of fly ash in manufacturing of BCS brick can reduce the problem with handling of fly ash to some extent.

Chapter 8: Scope for future work

1) Warpage test of bricks can also be performed to assess its warping nature
2) Other industrial wastes such as bottom ash, pond ash, GGBS, silica fumes and copper slag, rice husk ash can also be used to assess the compatibility of black cotton soil with them.
3) A feasibility study can be done to manufacture any other type of aesthetic elements/members by using black cotton soil and fly ash
4) Further work can be carried out to develop the technology to improve upon the swelling potential of black cotton soil.
5) A study can be carried out to find the route cause for swelling propensity of black cotton soil.

PRINCIPAL
Navodaya Institute of Technology
RAICHUR-584 103

CONCRETE TECHNOLOGY (COMMON TO CV/TR/CTM)

Sub Code	:	**10 CV 42**	**IA Marks**	:	**25**
Hrs/ Week	:	**04**	**Exam Hours**	:	**03**
Total Hrs.	:	**52**	**Exam Marks**	:	**100**

PART – A

Unit- 1 19
ement, Chemical composition, hydration of cement, Types of cement, manufacture of OPC by wet and dry, process (flow charts only) Testing of cement - Field testing, Fineness by sieve test and Blaine's air permeability test, Normal consistency, testing time, soundness, Compression strength of cement and grades of cement, Quality of mixing water. –7 Hours

Unit-2
Fine aggregate - grading, analysis, Specify gravity, bulking, moisture content, deleterious materials. Coarse aggregate – Importanc e of size, shape and texture.Grading of aggregates - Sieve analysis, specific gravity, Flakiness and elongation index, crushing, impact and abrasion tests. - 6 Hours

Unit-3
Workability - factors affecting workability, Measurement of workability - slump, flow tests, Compaction factor and vee-bee consistometer tests, Segregation and bleeding, Process of manufactures of concrete : Batching, Mixing, Transporting, Placing, Compaction, Curing. -7 Hours

Unit-4
Chemical admixtures - plasticizers, accelerators, retarders and air entraining agents, Mineral admixtures - Fly ash, Silica fumes and rice husk ash.
-6 Hours

Part-B

Unit-5
Factors affecting strength, w/c ratio, gel/space ratio, maturity concept, Effect of aggregate properties, relation between compressive strength, and tensile strength, bond strength, modulus of rupture, Accelerated curing, aggregate - cement bond strength, Testing of hardened concrete - compressive strength, split tensile strength, Flexural strength, factors influencing strength test results. - 6Hours

Unit-6
Elasticity - Relation between modulus of elasticity and Strength, factors affecting modulus of elasticity, Poisson , Ratio, Shrinkage - plastic shrinkage and drying shrinkage, Factors affecting shrinkage, Creep - Measurement of creep, factors affecting creep, effect of creep, - 7 Hours

Unit-7
Durability - definition, significance, permeability, Sulphate attack, Chloride attack, carbonation, freezing and thawing, Factors contributing to cracks in concrete - plastic shrinkage, settlement cracks, construction joints, Thermal expansion, transition zone, structural design deficiencies, - 6 Hours

Unit-8
Concept of Concrete Mix design, variables in proportioning , exposure conditions, Procedure of mix design as per IS 10262-1982, Numerical examples of Mix Design - 7 Hours

TEXT BOOKS:
1. "Concrete Technology" - Theory and Practice, M.S.Shetty, S.Chand and Company, New Delhi, 2002.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (....)
RAICHUR-584 103

BASIC MATERIAL TESTING LAB
(COMMON TO CV/TR)

Sub Code	:	10 CVL 37	**IA Marks**	:	25
Hrs/ Week	:	03	**Exam Hours**	:	03
Total Hrs.	:	42	**Exam Marks**	:	50

1. Tension test on Mild steel and HYSD bars.
2. Compression test of Mild Steel, Cast iron and Wood.
3. Torsion test on Mild Steel circular sections
4. Bending Test on Wood Under two point loading
5. Shear Test on Mild steel.
6. Impact test on Mild Steel (Charpy & Izod)
7. Hardness tests on ferrous and non-ferrous metals – Brinell's, Rockwell and Vicker's
8. Test on Bricks and Tiles
9. Tests on Fine aggregates – Moisture content, Specif ic gravity, Bulk density, Sieve analysis and Bulking
10. Tests on Coarse aggregates – Absorption, Moisture c ontent, specific gravity, Bulk density and Sieve analysis
11. Demonstration of Strain gauges and Strain indicators

NOTE: All tests to be carried out as per relevant BIS Codes

REFERENCE BOOKS:

1. **Testing of Engineering Materials**, Davis, Troxell and Hawk, International Student Edition – McGraw Hill Book Co . New Delhi.
2. **Mechanical Testing of Materials",** Fenner, George Newnes Ltd. London.
3. **"Experimental Strength of Materials"** , Holes K A, English Universities Press Ltd. London.
4. **"Testing of Metallic Materials"** , Suryanarayana A K, Prentice Hall of India Pvt. Ltd. New Delhi.
5. **Relevant IS Codes**
6. **"Material Testing Laboratory Manual"** , Kukreja C B- Kishore K. Ravi Chawla Standard Publishers & Distributors 1996.
7. **Concrete Manual,** M.L.Gambhir –Dhanpat Rai & Sons- New Delhi.

Scheme of Examination:

Group Experiments: Tension, Compression Torsion and Bending Tests Individual Experiments: Remaining tests

Two questions are to be set – one from group experi ments and the other as individual experiment.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (III),
RAICHUR-584 103

DESIGN OF RCC STRUCTURAL ELEMENTS

Subject Code	: 10CV52	IA Marks	: 25
No. of Lecture Hours/Week	: 04	Exam Hours	: 03
Total No. of Lecture Hours	: 52	Exam Marks	: 100

PART - A

UNIT - 1

GENERAL FEATURES OF REINFORCED CONCRETE: Introduction, Design Loads, Materials for Reinforced Concrete and Code requirements. Design Philosophy – Limit State Design principles. Philosophy of limit state design, Principles of limit states, Factor of Safety, Characteristic and design loads, Characteristic and design strength.

6 Hours

UNIT - 2

PRINCIPLES OF LIMIT STATE DESIGN AND ULTIMATE STRENGTH OF R.C. SECTION: General aspects of Ultimate strength, Stress block parameters for limit state of collapse, Ultimate flexural strength of singly reinforced rectangular sections, Ultimate flexural strength of doubly reinforced rectangular sections, Ultimate flexural strength of flanged sections, Ultimate shear strength of RC sections, Ultimate torsional strength of RC sections, Concepts of development length and anchorage, Analysis examples of singly reinforced, doubly reinforced, flanged sections, shear strength and development length.

7 Hours

UNIT - 3

FLEXURE AND SERVICEABILITY LIMIT STATES: General Specification for flexure design of beams-practical requirements, size of beam, cover to reinforcement-spacing of bars. General aspects of serviceability-Deflection limits in IS: 456 – 2000- Calculation of deflection (Theoretical method), Cracking in structural concrete members, Calculation of deflections and crack width.

NIT - 4

DESIGN OF BEAMS: Design procedures for critical sections for moment and shears. Anchorages of bars, check for development length, Reinforcement requirements, Slenderness limits for beams to ensure lateral stability, Design examples for Simply supported and Cantilever beams for rectangular and flanged sections.

8 Hours

PART - B

UNIT - 5

DESIGN OF SLABS: General consideration of design of slabs, Rectangular slabs spanning one direction, Rectangular slabs spanning in two directions for various boundary conditions. Design of simply supported, cantilever and continuous slabs as per IS: 456 – 2000.

8 Hours

UNIT - 6

DESIGN OF COLUMNS: General aspects, effective length of column, loads on columns, slenderness ratio for columns, minimum eccentricity, design of short axially loaded columns, design of column subject to combined axial load and uniaxial moment and biaxial moment using SP – 16 charts.

5 Hours

UNIT - 7

DESIGN OF FOOTINGS: Introduction, load for footing, Design basis for limit state method, Design of isolated rectangular footing for axial load and uniaxial moment, design of pedestal.

6 Hours

UNIT - 8

DESIGN OF STAIR CASES: General features, types of stair case, loads on stair cases, effective span as per IS code provisions, distribution of loading on stairs, Design of stair cases. With waistslabs.

6 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

GEOTECHNICAL ENGINEERING – I

Subject Code	: 10CV54	IA Marks	: 25
No. of Lecture Hours/Week	: 04	Exam Hours	: 03
Total No. of Lecture Hours	: 52	Exam Marks	: 100

PART - A

UNIT- 1

INTRODUCTION: History of soil mechanics, Definition, origin and formation of soil. Phase Diagram, Voids ratio, Porosity, Percentage Air Voids, Air content, Degree of saturation, Water content, Specific Gravity of soil solids and soil mass, Densities and Unit weights - Bulk, Dry, Saturated & Submerged and their inter relationships.

6 Hours

UNIT - 2

INDEX PROPERTIES OF SOIL AND THEIR DETERMINATION:

Index Properties of soil- Water content , Specific Gravity, Particle size distribution, Relative Density, Consistency limits and indices, in-situ density, Activity of Clay, Laboratory methods of determination of index properties of soil: Water content (Oven Drying method & Rapid Moisture method), Specific gravity of soil solids (Pycnometer and density bottle method), Particle size distribution (Sieve analysis and Hydrometer analysis only), Liquid Limit- (Casagrande and Cone penetration methods), Plastic limit and shrinkage limit.

7 Hours

UNIT - 3

CLASSIFICATION OF SOILS: Purpose of soil classification, Particle size classification – MIT classification and IS classifi cation, Textural classification. IS classification - Plasticity chart and its importance, Field identification of soils.

CLAY MINERALOGY AND SOIL STUCTURE: Single grained, honey combed, flocculent and dispersed structures, Valence bonds, Soil-Water system, Electrical diffuse double layer, adsorbed water, base-exchange capacity, Isomorphous substitution. Common clay minerals in soil and their structures- Kaolinite, Illite and Montmorillonite.

8 Hours

UNIT - 4

FLOW OF WATER THROUGH SOILS: Darcy's law- assumption and validity, coefficient of permeability and its determination (laboratory and field), factors affecting permeability, permeability of stratified soils, Seepage

velocity, Superficial velocity and coefficient of percolation, quick sand phenomena, Capillary Phenomena.

6 Hours

PART - B

UNIT - 5

SHEAR STRENGTH OF SOIL: Concept of shear strength, Mohr-coulomb theory, conventional and modified failure envelops, Effective stress concept-total stress, effective stress and Neutral stress, Concept of pore pressure, Total and effective shear strength parameters, factors affecting shear strength of soils, Sensitivity and Thixotropy of clay.

7 Hours

UNIT - 6

COMPACTION OF SOIL: Definition, Principle of compaction, Standard and Modified proctor's compaction tests, factors affecting compaction, effect of compaction on soil properties, Field compaction control – compactive effort & method, lift thickness and number of passes, Proctor's needle, Compacting equipment.

6 Hours

UNIT - 7

CONSOLIDATION OF SOIL: Definition, Mass-spring analogy, Terzaghi's one dimensional consolidation theory- assumption and limitations (no derivation), Normally consolidated, under

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 2/6/2014
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

GEOTECHNICAL ENGINEERING LABORATORY

Subject Code	: 10CVL67	IA Marks	: 25
No. of Practical Hours/Week	: 03	Exam Hours	: 03
Total No. of Practical Hours	: 42	Exam Marks	: 50

1. Identification of gravel type, sand type, silt type and clay types soils, Tests for determination of Specific gravity (for coarse and fine grained soils) and Water content (Oven drying method).

   3 Hours

2. Grain size analysis of soil sample (sieve analysis).

   3 Hours

3. In situ density by core cutter and sand replacement methods.

   3 Hours

4. Consistency Limits – Liquid Limit (Casagrande and Cone Penetration Methods), plastic limit and shrinkage limit.

   3 Hours

5. Standard Proctor Compaction Test and Modified Proctor Compaction Test.

   3 Hours

6. Coefficient of permeability by constant head and variable head methods.

   3 Hours

7. Strength Tests
   a. Unconfined Compression Test
   b. Direct Shear Test **3 Hours**
   c. Triaxial Compression Test (undrained)
   3 Hours

8. Consolidation Test- Determination of compression index and coefficient of consolidation.

   3 Hours

9. Laboratory vane shear test **3 Hours**

10. Determination of CBR value **3 Hours**

11. a) Demonstration of miscellaneous equipments such as Augers, Samplers, Rapid Moisture meter, Proctor's needle.
    b) Demonstration of Hydrometer Test.
    c) Demonstration of Free Swell Index and Swell Pressure Test
    d) Demonstration of determination of relative density of sands. **Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL 2/6/2020
Navodaya Institute of Technology
RAICHUR-584 103

2020/6/18 18:35

ESTIMATION & VALUATION

Subject Code	: 10CV73	IA Marks	: 25
No. of Lecture Hours/Week	: 04	Exam Hours	: 03
Total No. of Lecture Hours	: 52	Exam Marks	: 100

PART - A

ESTIMATION: Study of various drawings with estimates, important terms, units of measurement, abstract Methods of taking out quantities and cost – center line method, long and short wall method or crossing method. Preparation of detailed and abstract estimates for the following Civil Engineering works – Buildings – RCC framed structur es with flat, sloped RCC roofs with all Building components.

16 Hours

PART - B

ESTIMATE: Different type of estimates, approximate methods of estimating buildings, cost of materials. Estimation of wooden joineries such as doors, windows & ventilators.

5 Hours

ESTIMATES: Steel truss (Fink and Howe truss), manhole and septic tanks, RCC Culverts.

6 Hours

SPECIFICATIONS: Definition of specifications, objective of writing specifications, essentials in specifications, general and detail specifications of common item of works in buildings.

5 Hours

PART - C

RATE ANALYSIS: Definition and purpose. Working out quantities and rates for the following standard items of works – earth work in different types of soils, cement concrete of different mixes, bricks and stone masonry, flooring, plastering, RCC works, centering and form work for different RCC items, wood and steel works for doors, windows and ventilators.

6 Hours

MEASUREMENT OF EARTHWORK FOR ROADS: Methods for computation of earthwork – cross sections – mid sec tion formula or average

end area or mean sectional area, trapezoidal & prismoidal formula with and without cross slopes.

6 Hours

CONTRACTS: Types of contract – essentials of contract agreeme nt – legal aspects, penal provisions on breach of contract. Definition of the terms – Tender, earnest money deposit, security deposit, tender forms, documents and types. Acceptance of contract documents. Termination of contract, completion certificate, quality control, right of contractor, refund of deposit. Administrative approval – Technical sanction. Nomin al muster roll, measurement books – procedure for recording and che cking measurements – preparation of bills.
Valuation- Definitions of various terms, method of valuation, Freehold & Leasehold properties, Sinking fund, depreciation and method of estimating depreciation, Outgoings.

8 Hours

REFERENCE BOOKS:

1. **Estimating & Costing**, B. N. Dutta, Chand Publisher
2. **Quantity Surveying**- P.L. Basin S. Chand : New Delhi.
3. **Estimating & Specification** - S.C. Rangwala :: Charotar publishing house, Anand.
4. **Text book of Estimating & Costing**- G.S. Birde, Dhanpath Rai and sons : New Delhi.
5. **A text book on Estimating, Costing and Accounts**- D.D. Kohli and R.C. Kohli S. Chand : New Delhi.
6. **Contracts and Estimates,** B. S. Patil, University Press, 2006.

CONCRETE AND HIGHWAY MATERIALS LABORATORY

Subject Code	: 10CVL78	IA Marks	: 25
No. of Practical Hours/Week	: 03	Exam Hours	: 03
Total No. of Practical Hours	: 42	Exam Marks	: 50

PART - A

CEMENT: Normal Consistency, Setting time, Soundness by Autoclave method, Compression strength test and Air permeability test for fineness, Specific gravity of cement.

FRESH CONCRETE: Workability – slump, Compaction factor and Vee Bee tests.

HARDENED CONCRETE: Compression strength and Split tensile tests. Test on flexural strength of RCC beams, Permeability of concrete.

PART - B

SOIL: Density of Soil by Sand replacement method, CBR Text.

AGGREGATES: Crushing, abrasion, impact and Shape tests (Flaky, Elongation, Angularity number) Specific gravity and water absorption.

BITUMINOUS MATERIALS AND MIXES: Specific Gravity, Penetration,Ductility, Softening point, Flash and fire point, Viscosity, proportioning of aggregate mixes by Rothfutch Method, Marshall Stability tests.

REFERENCE BOOK:

1. Relevant IS Codes and IRC Codes.
2. **Highway Material Testing Laboratory Manual** by Khanna S K and Justo, – CEG Nemi Chand & Bros.
3. M. L. Gambhir : Concrete Manual : Dhanpat Rai & sons New – Delhi.

****

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL

VIII -SEMESTER

ADVANCED CONCRETE TECHNOLOGY

Subject Code	: 10CV81	IA Marks	: 25
No. of Lecture Hours/Week	: 04	Exam Hours	: 03
Total No. of Lecture Hours	: 52	Exam Marks	: 100

PART - A

UNIT - 1

Importance of Bogue's compounds, Structure of a Hydrated Cement Paste, Volume of hydrated product, porosity of paste and concrete, transition Zone, Elastic Modulus, factors affecting strength and elasticity of concrete, Rheology of concrete in terms of Bingham's parameter.

7 Hour

UNIT - 2

CHEMICAL ADMIXTURES- Mechanism of chemical admixture, Plasticizers and super Plasticizers and their effect on concrete property in fresh and hardened state, Marsh cone test for optimum dosage of super plasticizer, retarder, accelerator, Air-entraining admixtures, new generation superplasticiser.

MINERAL ADMIXTURE-Fly ash, Silica fume, GCBS, and their effect on concrete property in fresh state and hardened state.

6 Hours

UNIT - 3

MIX DESIGN - Factors affecting mix design, design of concrete mix by BIS method using IS10262 and current American (ACI)/ British (BS) methods. Provisions in revised IS10262-2004.

6 Hours

UNIT - 4

DURABILITY OF CONCRETE - Introduction, Permeability of concrete, chemical attack, acid attack, efflorescence, Corrosion in concrete. Thermal conductivity, thermal diffusivity, specific heat. Alkali Aggregate Reaction, IS456-2000 requirement for durability.

7 Hours

PART - B

UNIT - 5

RMC concrete - manufacture, transporting, placing, precautions, Methods of concreting- Pumping, under water concreting, shotcrete, High volume fly ash concrete concept, properties, typical mix

Self compacting concrete concept, materials, tests, properties, application and Typical mix.

6 Hours

UNIT - 6

Fiber reinforced concrete - Fibers types and properties, Behavior of FRC in compression, tension including pre-cracking stage and post-cracking stages, behavior in flexure and shear, Ferro cement - materials, techniques of manufacture, properties and application

7 Hours

UNIT - 7

Light weight concrete-materials properties and types. Typical light weight concrete mix High density concrete and high performance concrete-materials, properties and applications, typical mix.

6 Hours

UNIT - 8

Test on Hardened concrete-Effect of end condition of specimen, capping, H/D ratio, rate of loading, moisture condition. Compression, tension and flexure tests. Tests on composition of hardened concrete-cement content, original w/c ratio. NDT tests concepts-Rebound hammer, pulse velocity methods.

7 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Computer Science Engineering

UNIT – 8 **6 Hours**

Group Codes: Decoding with Coset Leaders, Hamming Matrices

Rings and Modular Arithmetic: The Ring Structure – Definition and Examples, Ring Properties and Substructures, The Integers Modulo n

Text Book:

1. Ralph P. Grimaldi: Discrete and Combinatorial Mathematics, , 5th Edition, Pearson Education, 2004.
   (Chapter 3.1, 3.2, 3.3, 3.4, Appendix 3, Chapter 2, Chapter 4.1, 4.2, Chapter 5.1 to 5.6, Chapter 7.1 to 7.4, Chapter 16.1, 16.2, 16.3, 16.5 to 16.9, and Chapter 14.1, 14.2, 14.3).

Reference Books:

1. Kenneth H. Rosen: Discrete Mathematics and its Applications, 7th Edition, McGraw Hill, 2010.
2. Jayant Ganguly: A Treatise on Discrete Mathematical Structures, Sanguine-Pearson, 2010.
3. D.S. Malik and M.K. Sen: Discrete Mathematical Structures: Theory and Applications, Cengage Learning, 2004.
4. Thomas Koshy: Discrete Mathematics with Applications, Elsevier, 2005, Reprint 2008.

DATA STRUCTURES WITH C
(Common to CSE & ISE)

Subject Code: 10CS35	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT - 1 **8 Hours**

BASIC CONCEPTS: Pointers and Dynamic Memory Allocation, Algorithm Specification, Data Abstraction, Performance Analysis, Performance Measurement

UNIT - 2 **6 Hours**

ARRAYS and STRUCTURES: Arrays, Dynamically Allocated Arrays, Structures and Unions, Polynomials, Sparse Matrices, Representation of Multidimensional Arrays

UNIT - 3 **6 Hours**

STACKS AND QUEUES: Stacks, Stacks Using Dynamic Arrays, Queues, Circular Queues Using Dynamic Arrays, Evaluation of Expressions, Multiple Stacks and Queues.

UNIT - 4 **6 Hours**

LINKED LISTS: Singly Linked lists and Chains, Representing Chains in C, Linked Stacks and Queues, Polynomials, Additional List operations, Sparse Matrices, Doubly Linked Lists

PART - B

UNIT - 5 **6 Hours**

TREES – 1: Introduction, Binary Trees, Binary Tree Traversals, Threaded Binary Trees, Heaps.

UNIT - 6

6 Hours

TREES – 2, GRAPHS: Binary Search Trees, Selection Trees, Forests, Representation of Disjoint Sets, Counting Binary Trees, The Graph Abstract Data Type.

UNIT - 7 **6 Hours**

PRIORITY QUEUES Single- and Double-Ended Priority Queues, Leftist Trees, Binomial Heaps, Fibonacci Heaps, Pairing Heaps.

UNIT - 8 **8 Hours**

EFFICIENT BINARY SEARCH TREES: Optimal Binary Search Trees, AVL Trees, Red-Black Trees, Splay Trees.

Text Book:

1. Horowitz, Sahni, Anderson-Freed: Fundamentals of Data Structures in C, 2nd Edition, Universities Press, 2007.
   (Chapters 1, 2.1 to 2.6, 3, 4, 5.1 to 5.3, 5.5 to 5.11, 6.1, 9.1 to 9.5, 10)

Reference Books:

1. Yedidyah, Augenstein, Tannenbaum: Data Structures Using C and C++, 2nd Edition, Pearson Education, 2003.
2. Debasis Samanta: Classic Data Structures, 2nd Edition, PHI, 2009.
3. Richard F. Gilberg and Behrouz A. Forouzan: Data Structures A Pseudocode Approach with C, Cengage Learning, 2005.

Subject Code: 10CS44	I.A. Marks : 25
Hours/Week : 04	Exam Hours: 03
Total Hours : 52	Exam Marks: 100

PART – A

UNIT – 1 **6 Hours**

The Unix Operating System, The UNIX architecture and Command Usage, The File System

UNIT - 2 **6 Hours**

Basic File Attributes, the vi Editor

UNIT – 3 **7 Hours**

The Shell, The Process, Customizing the environment

UNIT - 4 **7 Hours**

More file attributes, Simple filters

PART – B

UNIT – 5 **6 Hours**

Filters using regular expressions,

UNIT – 6 **6 Hours**

Essential Shell Programming

UNIT - 7 **7 Hours**

awk – An Advanced Filter

UNIT - 8 **7 Hours**

perl - The Master Manipulator

Text Book:

1. Sumitabha Das: UNIX – Concepts and Applications, 4th Edition, Tata McGraw Hill, 2006. (Chapters 1.2, 2, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 18, 19)

Reference Books:

1. Behrouz A. Forouzan and Richard F. Gilberg: UNIX and Shell Programming, Cengage Learning, 2005.
2. M.G. Venkateshmurthy: UNIX & Shell Programming, Pearson Education, 2005.

(Common to CSE & ISE)

Subject Code: 10CS45	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART A

UNIT – I **7 Hours**

Introduction, Microprocessor Architecture – 1: A Historical Background, The Microprocessor-Based Personal Computer Systems.

The Microprocessor and its Architecture: Internal Microprocessor Architecture, Real Mode Memory Addressing.

UNIT – 2 **7 Hours**

Microprocessor Architecture – 2, Addressing Modes: Introduction to Protected Mode Memory Addressing, Memory Paging, Flat Mode Memory Addressing Modes: Data Addressing Modes, Program Memory Addressing Modes, Stack Memory Addressing Modes

UNIT – 3 **6 Hours**

Programming – 1: Data Movement Instructions: MOV Revisited, PUSH/POP, Load-Effective Address, String Data Transfers, Miscellaneous Data Transfer Instructions, Segment Override Prefix, Assembler Details.

Arithmetic and Logic Instructions: Addition, Subtraction and Comparison, Multiplication and Division.

UNIT - 4 **6 Hours**

Programming – 2: Arithmetic and Logic Instructions (continued): BCD and ASCII Arithmetic, Basic Logic Instructions, Shift and Rotate, String Comparisons.

Program Control Instructions: The Jump Group, Controlling the Flow of the Program, Procedures, Introduction to Interrupts, Machine Control and Miscellaneous Instructions.

PART B

UNIT - 5 **6 Hours**

Programming – 3: Combining Assembly Language with C/C++: Using Assembly Language with C/C++ for 16-Bit DOS Applications and 32-Bit Applications

Modular Programming, Using the Keyboard and Video Display, Data Conversions, Example Programs

3. Uresh Vahalia: UNIX Internals: The New Frontiers, Pearson Education, 2001.

COMPILER DESIGN

Subject Code: 10CS63	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **8 Hours**

Introduction, Lexical analysis: Language processors; The structure of a Compiler; The evolution pf programming languages; The science of building a Compiler; Applications of compiler technology; Programming language basics.

Lexical analysis: The Role of Lexical Analyzer; Input Buffering; Specifications of Tokens; Recognition of Tokens.

UNIT – 2 **6 Hours**

Syntax Analysis – 1: Introduction; Context-free Grammars; Writing a Grammar. Top-down Parsing; Bottom-up Parsing.

UNIT – 3 **6 Hours**

Syntax Analysis – 2: Top-down Parsing; Bottom-up Parsing.

UNIT – 4 **6 Hours**

Syntax Analysis – 3: Introduction to LR Parsing: Simple LR; More powerful LR parsers (excluding Efficient construction and compaction of parsing tables) ; Using ambiguous grammars; Parser Generators.

PART – B

UNIT – 5 **7 Hours**

Syntax-Directed Translation: Syntax-directed definitions; Evaluation orders for SDDs; Applications of syntax-directed translation; Syntax-directed translation schemes.

UNIT – 6 **6 Hours**

Intermediate Code Generation: Variants of syntax trees; Three-address code; Translation of expressions; Control flow; Back patching; Switch-statements; Procedure calls.

UNIT – 7 **6 Hours**

Run-Time Environments: Storage Organization; Stack allocation of space; Access to non-local data on the stack; Heap management; Introduction to garbage collection.

UNIT – 8 **7 Hours**

Code Generation: Issues in the design of Code Generator; The Target Language; Addresses in the target code; Basic blocks and Flow graphs; Optimization of basic blocks; A Simple Code Generator

Text Books:

1. Alfred V Aho, Monica S.Lam, Ravi Sethi, Jeffrey D Ullman: Compilers- Principles, Techniques and Tools, 2nd Edition, Pearson Education, 2007.
   (Chapters 1, 3.1 to 3.4, 4 excluding 4.7.5 and 4.7.6, 5.1 to 5.4, 6.1, 6.2, 6.4, 6.6, 6.7 to 6.9, 7.1 to 7.5, 8.1 to 8.6.)

Reference Books:

1. Charles N. Fischer, Richard J. leBlanc, Jr.: Crafting a Compiler with C, Pearson Education, 1991.
2. Andrew W Apple: Modern Compiler Implementation in C, Cambridge University Press, 1997.
3. Kenneth C Louden: Compiler Construction Principles & Practice, Cengage Learning, 1997.

COMPUTER NETWORKS - II

Subject Code: 10CS64	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART - A

UNIT - 1 **6 Hours**

Packet Switching Networks - 1: Network services and internal network operation, Packet network topology, Routing in Packet networks, Shortest path routing: Bellman-Ford algorithm.

UNIT – 2 **6 Hours**

Packet Switching Networks – 2: Shortest path routing (continued), Traffic management at the Packet level, Traffic management at Flow level, Traffic management at flow aggregate level.

Reference Book:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers

ELECTRONIC CIRCUITS
(Common to CSE & ISE)

Subject Code: 10CS32	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART - A

UNIT - 1 **7 Hours**

Transistors, UJTs, and Thyristors: Operating Point, Common-Emitter Configuration, Thermal Runaway, Transistor Switch, Unijunction Transistors, SCR.

UNIT - 2 **6 Hours**

Field Effect Transistors: Bipolar Junction Transistors versus Field Effect Transistors, Junction Field Effect Transistors, Metal Oxide Field Effect Transistors, Differences between JFETs and MOSFETs, Handling MOSFETs, Biasing MOSFETs, FET Applications, CMOS Devices, Insulated Gate Bipolar Transistors (IGBTs)

UNIT - 3 **6 Hours**

Optoelectronic Devices: Introduction, Photosensors, Photoconductors, Photodiodes, Phototransistors, Light-Emitting Diodes, Liquid Crystal Displays, Cathode Ray Tube Displays, Emerging Display Technologies, Optocouplers

UNIT - 4 **7 Hours**

Small Signal Analysis of Amplifiers: Amplifier Bandwidth: General Frequency Considerations, Hybrid h-Parameter Model for an Amplifier, Transistor Hybrid Model, Analysis of a Transistor Amplifier using complete h-Parameter Model, Analysis of a Transistor Amplifier Configurations using Simplified h-Parameter Model (CE configuration only), Small-Signal

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (N.I.T.)
RAICHUR-584 103

Analysis of FET Amplifiers, Cascading Amplifiers, Darlington Amplifier, Low-Frequency Response of Amplifiers (BJT amplifiers only).

PART - B

UNIT - 5 **6 Hours**

Large Signal Amplifiers, Feedback Amplifier: Classification and characteristics of Large Signal Amplifiers, Feedback Amplifiers: Classification of Amplifiers, Amplifier with Negative Feedback, Advantages of Negative Feedback, Feedback Topologies, Voltage-Series (Series-Shunt) Feedback, Voltage-Shunt (Shunt-Shunt) Feedback, Current-Series (Series-Series) Feedback, Current-Shunt (Shunt-Series) Feedback.

UNIT - 6 **7 Hours**

Sinusoidal Oscillators, Wave-Shaping Circuits: Classification of Oscillators, Conditions for Oscillations: Barkhausen Criterion, Types of Oscillators, Crystal Oscillator, Voltage-Controlled Oscillators, Frequency Stability.

Wave-Shaping Circuits: Basic RC Low-Pass Circuit, RC Low-Pass Circuit as Integrator, Basic RC High-Pass Circuit, RC High-Pass Circuit as Differentiator, Multivibrators, Integrated Circuit (IC) Multivibrators.

UNIT - 7 **7 Hours**

Linear Power Supplies, Switched mode Power Supplies: Linear Power Supplies: Constituents of a Linear Power Supply, Designing Mains Transformer; Linear IC Voltage Regulators, Regulated Power Supply Parameters.

Switched Mode Power Supplies: Switched Mode Power Supplies, Switching Regulators, Connecting Power Converters in Series, Connecting Power Converters in Parallel

UNIT - 8 **6 Hours**

Operational Amplifiers: Ideal Opamp versus Practical Opamp, Performance Parameters, Some Applications: Peak Detector Circuit, Absolute Value Circuit, Comparator, Active Filters, Phase Shifters, Instrumentation Amplifier, Non-Linear Amplifier, Relaxation Oscillator, Current-To-Voltage Converter, Voltage-To-Current Converter, Sine Wave Oscillators.

Text Book:

1. Anil K Maini, Varsha Agarwal: Electronic Devices and Circuits, Wiley, 2009.
   (4.1, 4.2, 4.7, 4.8, 5.1 to 5.3, 5.5, 5.6, 5.8, 5.9, 5.13, 5.14, 6.1, 6.3, 7.1 to 7.5, 7.10 to 7.14, Listed topics only from 8, 10.1, 11, 12.1, 12.2, 12.3, 12.5, 13.1 to 13.6, 13.9, 13.10, 14.1, 14.2, 14.6, 14.7, 15.1, 15.5 to 15.7. 16.3, 16.4, 17.12 to 17.22)

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Computer Science & Engineering

PRINCIPAL
Navodaya Institute of Technology
RAICHUR-584 103

LEX and YACC, LEX and Hand- Written Lexers, Using LEX - Regular Expression, Examples of Regular Expressions, A Word Counting Program, Parsing a Command Line.

UNIT – 8 **6 Hours**

Lex and Yacc - 2: Using YACC – Grammars, Recursive Rules, Shift/Reduce Parsing, What YACC Cannot Parse, A YACC Parser - The Definition Section, The Rules Section, Symbol Values and Actions, The LEXER, Compiling and Running a Simple Parser, Arithmetic Expressions and Ambiguity, Variables and Typed Tokens.

Text Books:

1. Leland.L.Beck: System Software, 3rd Edition, Pearson Education, 1997.
   (Chapters 1.1 to 1.3, 2 (except 2.5.2 and 2.5.3), 3 (except 3.5.2 and 3.5.3), 4 (except 4.4.3))
2. John.R.Levine, Tony Mason and Doug Brown: Lex and Yacc, O'Reilly, SPD, 1998.
   (Chapters 1, 2 (Page 2-42), 3 (Page 51-65))

Reference Books:

1. D.M.Dhamdhere: System Programming and Operating Systems, 2nd Edition, Tata McGraw - Hill, 1999.

OPERATING SYSTEMS

Subject Code: 10CS53	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **6 Hours**

Introduction to Operating Systems, System structures: What operating systems do; Computer System organization; Computer System architecture; Operating System structure; Operating System operations; Process management; Memory management; Storage management; Protection and security; Distributed system; Special-purpose systems; Computing environments.Operating System Services; User - Operating System interface; System calls; Types of system calls; System programs; Operating System design and implementation; Operating System structure; Virtual machines; Operating System generation; System boot.

Head of Department
Computer Science & Engineering
Navodaya Institute of Technology

PRINCIPAL
Navodaya Institute of Technology
RAICHUR-584 103

UNIT – 2 **7 Hours**

Process Management: Process concept; Process scheduling; Operations on processes; Inter-process communication. Multi-Threaded Programming: Overview; Multithreading models; Thread Libraries; Threading issues. Process Scheduling: Basic concepts; Scheduling criteria; Scheduling algorithms; Multiple-Processor scheduling; Thread scheduling.

UNIT – 3 **7 Hours**

Process Synchronization : Synchronization: The Critical section problem; Peterson's solution; Synchronization hardware; Semaphores; Classical problems of synchronization; Monitors.

UNIT – 4 **6 Hours**

Deadlocks: Deadlocks: System model; Deadlock characterization; Methods for handling deadlocks; Deadlock prevention; Deadlock avoidance; Deadlock detection and recovery from deadlock.

PART – B

UNIT – 5 **7 Hours**

Memory Management: Memory Management Strategies: Background; Swapping; Contiguous memory allocation; Paging; Structure of page table; Segmentation. Virtual Memory Management: Background; Demand paging; Copy-on-write; Page replacement; Allocation of frames; Thrashing.

UNIT – 6 **7 Hours**

File System, Implementation of File System: File System: File concept; Access methods; Directory structure; File system mounting; File sharing; Protection. Implementing File System: File system structure; File system implementation; Directory implementation; Allocation methods; Free space management

UNIT – 7 **6 Hours**

Secondary Storage Structures, Protection : Mass storage structures; Disk structure; Disk attachment; Disk scheduling; Disk management; Swap space management. Protection: Goals of protection, Principles of protection, Domain of protection, Access matrix, Implementation of access matrix, Access control, Revocation of access rights, Capability-Based systems.

UNIT – 8 **6 Hours**

Case Study: The Linux Operating System: Linux history; Design principles; Kernel modules; Process management; Scheduling; Memory management; File systems, Input and output; Inter-process communication.

COMPUTER ORGANIZATION

Subject Code: 10CS46	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT - 1 **6 Hours**

Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement, Historical Perspective

Machine Instructions and Programs: Numbers, Arithmetic Operations and Characters, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing,

UNIT - 2 **7 Hours**

Machine Instructions and Programs *contd.*: Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions

UNIT - 3 **6 Hours**

Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses

UNIT - 4 **7 Hours**

Input/Output Organization *contd.*: Interface Circuits, Standard I/O Interfaces – PCI Bus, SCSI Bus, USB

PART – B

UNIT - 5 **7 Hours**

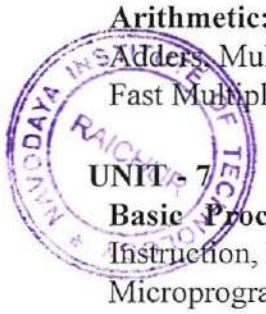
Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations, Virtual Memories, Secondary Storage

UNIT - 6 **7 Hours**

Arithmetic: Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers, Signed Operand Multiplication, Fast Multiplication, Integer Division, Floating-point Numbers and Operations

UNIT - 7 **6 Hours**

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Microprogrammed Control



Head of Department
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT - 8 **6 Hours**

Multicores, Multiprocessors, and Clusters: Performance, The Power Wall, The Switch from Uniprocessors to Multiprocessors, Amdahl's Law, Shared Memory Multiprocessors, Clusters and other Message Passing Multiprocessors, Hardware Multithreading, SISD, IMD, SIMD, SPMD, and Vector.

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002. (Listed topics only from Chapters 1, 2, 4, 5, 6, 7)
2. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009. (Listed topics only)

Reference Books:

1. William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
2. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

Head of Department
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

V SEMESTER

SOFTWARE ENGINEERING

Subject Code: 10IS51	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **6 Hours**

Overview: Introduction: FAQ's about software engineering, Professional and ethical responsibility.

Socio-Technical systems: Emergent system properties; Systems engineering; Organizations, people and computer systems; Legacy systems.

UNIT – 2 **6 Hours**

Critical Systems, Software Processes: Critical Systems: A simple safety-critical system; System dependability; Availability and reliability.

Software Processes: Models, Process iteration, Process activities; The Rational Unified Process; Computer Aided Software Engineering.

UNIT – 3 **7 Hours**

Requirements: Software Requirements: Functional and Non-functional requirements; User requirements; System requirements; Interface specification; The software requirements document.

Requirements Engineering Processes: Feasibility studies; Requirements elicitation and analysis; Requirements validation; Requirements management.

UNIT – 4 **7 Hours**

System models, Project Management: System Models: Context models; Behavioral models; Data models; Object models; Structured methods.

Project Management: Management activities; Project planning; Project scheduling; Risk management

PART - B

UNIT – 5 **7 Hours**

Software Design: Architectural Design: Architectural design decisions; System organization; Modular decomposition styles; Control styles.

Object-Oriented design: Objects and Object Classes; An Object-Oriented design process; Design evolution.

UNIT – 6 **6 Hours**

Development: Rapid Software Development: Agile methods; Extreme programming; Rapid application development.
Software Evolution: Program evolution dynamics; Software maintenance; Evolution processes; Legacy system evolution.

UNIT – 7 **7 Hours**

Verification and Validation: Verification and Validation: Planning; Software inspections; Automated static analysis; Verification and formal methods.
Software testing: System testing; Component testing; Test case design; Test automation.

UNIT – 8 **6 Hours**

Management: Managing People: Selecting staff; Motivating people; Managing people; The People Capability Maturity Model.
Software Cost Estimation: Productivity; Estimation techniques; Algorithmic cost modeling, Project duration and staffing.

Text Books:

1. Ian Sommerville: Software Engineering, 8th Edition, Pearson Education, 2007.
   (Chapters-: 1, 2, 3, 4, 5, 6, 7, 8, 11, 14, 17, 21, 22, 23, 25, 26)

Reference Books:

1. Roger.S.Pressman: Software Engineering-A Practitioners approach, 7th Edition, Tata McGraw Hill, 2007.
2. Pankaj Jalote: An Integrated Approach to Software Engineering, Wiley India, 2009.

SYSTEM SOFTWARE

Subject Code: 10CS52	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **6 Hours**

Machine Architecture: Introduction, System Software and Machine Architecture, Simplified Instructional Computer (SIC) - SIC Machine Architecture, SIC/XE Machine Architecture, SIC Programming Examples.

10. Write a C/C++ program to set up a real-time clock interval timer using the **alarm** API.

List of Experiments for Compiler Design: Design, develop, and execute the following programs.

11. Write a C program to implement the syntax-directed definition of "if E then S1" and "if E then S1 else S2". (Refer Fig. 8.23 in the text book prescribed for 06CS62 Compiler Design, Alfred V Aho, Ravi Sethi, and Jeffrey D Ullman: Compilers- Principles, Techniques and Tools, 2nd Edition, Pearson Education, 2007).

12. Write a yacc program that accepts a regular expression as input and produce its parse tree as output.

Note: In the examination *each* student picks one question from the lot of *all* 12 questions.

VII SEMESTER

OBJECT-ORIENTED MODELING AND DESIGN

Subject Code: 10CS71	**I.A. Marks : 25**
Hours/Week : 04	**Exam Hours: 03**
Total Hours : 52	**Exam Marks: 100**

PART – A

UNIT – 1 **7 Hours**

Introduction, Modeling Concepts, class Modeling: What is Object Orientation? What is OO development? OO themes; Evidence for usefulness of OO development; OO modeling history

Modeling as Design Technique: Modeling; abstraction; The three models.

Class Modeling: Object and class concepts; Link and associations concepts; Generalization and inheritance; A sample class model; Navigation of class models; Practical tips.

UNIT – 2 **6 Hours**

Advanced Class Modeling, State Modeling: Advanced object and class concepts; Association ends; N-ary associations; Aggregation; Abstract classes; Multiple inheritance; Metadata; Reification; Constraints; Derived data; Packages; Practical tips.

State Modeling: Events, States, Transitions and Conditions; State diagrams; State diagram behavior; Practical tips.

UNIT – 3 **6 Hours**

Advanced State Modeling, Interaction Modeling: Advanced State Modeling: Nested state diagrams; Nested states; Signal generalization; Concurrency; A sample state model; Relation of class and state models; Practical tips.

Interaction Modeling: Use case models; Sequence models; Activity models. Use case relationships; Procedural sequence models; Special constructs for activity models.

UNIT – 4 **7 Hours**

Process Overview, System Conception, Domain Analysis: Process Overview: Development stages; Development life cycle.

System Conception: Devising a system concept; Elaborating a concept; Preparing a problem statement.

Domain Analysis: Overview of analysis; Domain class model; Domain state model; Domain interaction model; Iterating the analysis.

PART – B

UNIT – 5 **7 Hours**

Application Analysis, System Design: Application Analysis: Application interaction model; Application class model; Application state model; Adding operations.

Overview of system design; Estimating performance; Making a reuse plan; Breaking a system in to sub-systems; Identifying concurrency; Allocation of sub-systems; Management of data storage; Handling global resources; Choosing a software control strategy; Handling boundary conditions; Setting the trade-off priorities; Common architectural styles; Architecture of the ATM system as the example.

UNIT – 6 **7 Hours**

Class Design, Implementation Modeling, Legacy Systems: Class Design: Overview of class design; Bridging the gap; Realizing use cases; Designing algorithms; Recursing downwards, Refactoring; Design optimization; Reification of behavior; Adjustment of inheritance; Organizing a class design; ATM example.

Implementation Modeling: Overview of implementation; Fine-tuning classes; Fine-tuning generalizations; Realizing associations; Testing.

Legacy Systems: Reverse engineering; Building the class models; Building the interaction model; Building the state model; Reverse engineering tips; Wrapping; Maintenance.

UNIT – 7 **6 Hours**

MANAGEMENT AND ENTREPRENEURSHIP

Subject Code: 10AL61 | **I.A. Marks : 25**
Hours/Week : 04 | **Exam Hours: 03**
Total Hours : 52 | **Exam Marks: 100**

PART–A

UNIT–1 7 Hours

MANAGEMENT: Introduction – Meaning – nature and characteristics of Management, Scope and functional areas of management – Management as a science, art or profession Management & Administration – Roles of Management, Levels of Management, Development of Management Thought – early management approaches – Modern management approaches.

UNIT–2 6 Hours

PLANNING: Nature, importance and purpose of planning process – Objectives – Types of plans (Meaning only) – Decision making – Importance of planning – steps in planning & planning premises – Hierarchy of plans.

UNIT–3 6 Hours

ORGANIZING AND STAFFING: Nature and purpose of organization – Principles of organization – Types of organization – Departmentation – Committees – Centralization Vs Decentralization of authority and responsibility – Span of control – MBO and MBE (Meaning only) Nature and importance of Staffing – Process of Selection & Recruitment (in brief)

UNIT–4 7 Hours

DIRECTING & CONTROLLING: Meaning and nature of directing – Leadership styles, Motivation Theories, Communication – Meaning and importance –Coordination,meaning and importance andTechniques ofCo – ordination.Meaning and steps in controlling – Essentials of a sound control system -Methods of establishing control (in brief)

PART-B-(ENTREPRENEURSHIP)

UNIT–5 6 Hours

ENTREPRENEUR: Meaning of Entrepreneur; Evolution of the Concept, Functions of an Entrepreneur, Types of Entrepreneur, Intrapreneur – an emerging Class. Concept of Entrepreneurship – Evolution of Entrepreneurship, Development of Entrepreneurship; Stages in entrepreneurial process; Role of entrepreneurs in Economic Development; Entrepreneurship in India; Entrepreneurship – its Barriers.

UNIT–6 6 Hours

SMALL SCALE INDUSTRY Definition; Characteristics; Need and rationale: Objectives; Scope; role of SSI in Economic Development. Advantages of SSI Steps to start an SSI – Government policy towards SSI; Different Policies of S.S.I.; Government Support for S.S.I. during 5 year plans, Impact of Liberalization, Privatization, Globalization on S.5.1., Effect of WTO/GATT Supporting Agencies of Government for S.5.!., Meaning; Nature of Support; Objectives; Functions; Types of Help; Ancillary Industry and Tiny Industry (Definition only).

Head of Department
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT–7 6 Hours

INSTITUTIONAL SUPPORT: Different Schemes; TECKSOK; KIADB; KSSIDC; KSIMC; DIC Single Window Agency: SISI; NSIC; SIDBI; KSFC.

UNIT–8 6 Hours

PREPARATION OF PROJECT : Meaning of Project; Project Identification; Project Selection; Project Report; Need and Significance of Report; Contents; formulation; Guidelines by Planning Commission for Project report; Network Analysis; Errors of Project Report; Project Appraisal. Identification of Business Opportunities: Market Feasibility Study; Technical Feasibility Study; Financial Feasibility Study & Social Feasibility Study

TEXT BOOKS:

1. Principles of Management – P.C. Tripathi, P.N. Reddy – Tata McGraw Hill, 2007.
2. Dynamics of Entrepreneurial Development & Management – Vasant Desai:, Himalaya Publishing House, 2007.
3. Entrepreneurship Development – Poornima M Charantimath – Small Business Enterprises, Pearson Education, 2006.

REFERENCE BOOKS:

1. Management Fundamentals Concepts, Application, Skill Development – Robert Lusier – ,Thompson, 2007.
2. Entrepreneurship Development – S. S. Khanka, S. Chand & Co., 2007.
3. Management – Stephen Robbins: 17th Edition, Pearson Education / PHI, 2003.
4. Web Sites for the Institutions listed in the Unit 7 on Institutional Support.

INSTITUTE OF TECH... RAICHUR

Head of Department 18/9/08
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

PRINCIPAL 18/9/08
Navodaya Institute of Technology (NITA)
RAICHUR-584 103

NET'S

NAVODAYA INSTITUTE OF TECHNOLOGY, RAICHUR

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

CERTIFICATE

This is to certify that the project and entitled "ANTI-THEFT INTIMATION OF VEHICLES OVER ANDROID SMARTPHONES" is bonafide work carried out by "ATITHI RANJAN JHA (3NA12CS005), SANJEEV K (3NA12CS021), PANKAJ KUMAR S (3NA12CS016), VIJAYALAKSHMI (3NA13CS404)" in partial fulfillment for the award of bachelor of engineering in "Computer Science & Engineering" of the Visvesvaraya Technological University, Belagavi, during the year 2015-2016. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the department library. The project has been approved as it satisfies the academic requirements in respect of the project prescribed for the said degree.

Prof. Rajashekar Reddy	Prof. Dr.A V N Krishna	Dr.Shivaprakash C K
PROJECT GUIDE	HOD	PRINCIPAL

Examiners **Signature with date**

1. ..... 13/06/16

2. ..... 13/6/16

Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ABSTRACT

GSM and GPS based vehicle location and tracking system will provide effective, real time vehicle location, mapping and reporting this information value and add by improving the level of service provided. A GPS-based vehicle tracking system will inform where your vehicle is and where it has been, how long it has been. The system uses geographic position and time information from the Global Positioning Satellites. This effective system for network system of vehicle tracking & locking facility from a remote end like control room or even vehicle owner's mobile. The operator can see the vehicle's current location in real time mode. Here the communication network is comparable to the cellular network in operation. In this project prototypes are made to illustrate the tracking and locking of vehicle.

CONTENTS

List of Figures

CHAPTER 1

Preamble

1.1 Introduction to vehicle tracking system

GSM and GPS based vehicle location and tracking system will provide effective, real time vehicle location, mapping and reporting this information value and added by improving the level of services provided. A GPS-based vehicle tracking system will inform where your vehicle is and where it has been, how long it has been. The system uses geographic position and time information from the Global Positioning Satellites. The system has an "On- Board Module" which resides in the vehicle to be tracked and a "Base Station" that monitors data from the various vehicles. The On-Board module consists of GPS receiver, a GSM modem.

A vehicle tracking system combines the installation of an electronic device in a vehicle, or fleet of vehicles, with purpose-designed computer software to enable the owner or a third party to track the vehicles location, collecting data in the process. Modern vehicle tracking systems commonly use Global Positioning System (GPS) technology for locating the Vehicle. To achieve automatic Vehicle Location system that can transmit the location information in real time. The information is transmitted to Tracking server using GSM/GPRS modem on GSM network by using SMS or using direct TCP/IP connection with Tracking server through GPRS. Tracking server also has GSM/GPRS modem that receives vehicle location information via GSM network and stores this information in database. This information is available to authorized users of the system via website over the internet.

The Project is not about the GPS, but about alternative technology which is much economical, simple and indigenous in design. There by resulting in an effective system for our own network system of vehicle tracking & locking facility from a remote end like control room or even vehicle owner's mobile.

1.5 Problem definition

The recent popularity in tracking of a vehicle system has encouraged the invention of GPS and GSM based vehicle tracking system. However the growth of the technology and the increase in need of the better vehicle security there is a strong emphasis on developing measures to prevent from theft and to avoid damage, this system has developed. Providing a secure environment to the vehicles is a challenge in recent security technology. So based on the challenges of providing security over vehicles this concept of gps/gsm based vehicle tracking and antitheft intimation along with locking the vehicle by the owner automatically by the remote based mode of wireless communication with the help android compatible application present in owner's mobile.

1.6 Objective

The objective of this project is to achieve a design of such system that can give information of the vehicle position every time when there's a request for it. The main goal of this project is to provide a security to the owner or the authorized user of the vehicle, by preventing the system from unauthorized access or the theft prevention of vehicle. It mainly involves the installation of the system with gps and gsm connectivity, inside a vehicle. The objective of this project is in following:

1. Input is the process of piezo electric mechanism of the accident sensor or the automatic start up of the system when engine of owner's vehicle becomes ON state.

2. It is achieved by the installation of tracking system in a vehicle.

3. When the vehicle starts it will automatically starts finding location details continuously.

CHAPTER 3

REQUIREMENT ANALYSIS

3.1 Software requirements

1. Compiler: Keil compiler UVersion 4
2. Language: Embedded C or Assembly

3.2 Hardware requirements

1. ARM 7 / Cortex M3
2. LCD
3. Relay Driver
4. Relays
5. Resistors
6. Capacitors
7. LEDs, Crystal
8. Diodes,
9. Transformer
10. Voltage Regulator
11. Push Button

CHAPTER 4

UML DIAGRAMS

4.1 USE CASE DIAGRAM

UML or Unified Modeling Language is "a standard notation for the modeling of real-world objects and systems". This language has various types of diagrams which are divided into two categories: structural diagrams and behavior diagrams. Structural diagrams emphasizes element that must be present in the system that is being modeled whereas behavioral diagrams illustrates what must happen in the system that is being modeled.

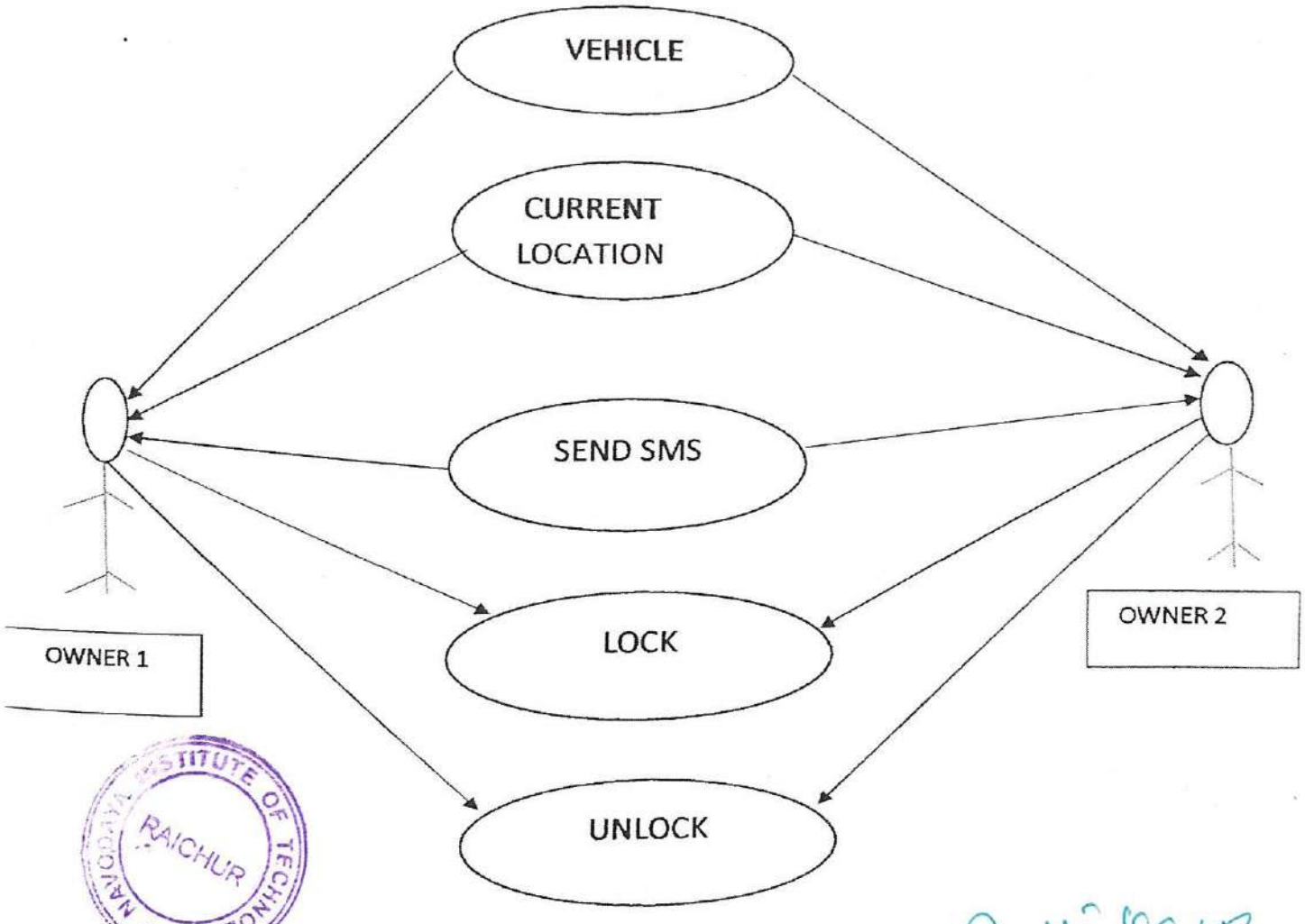
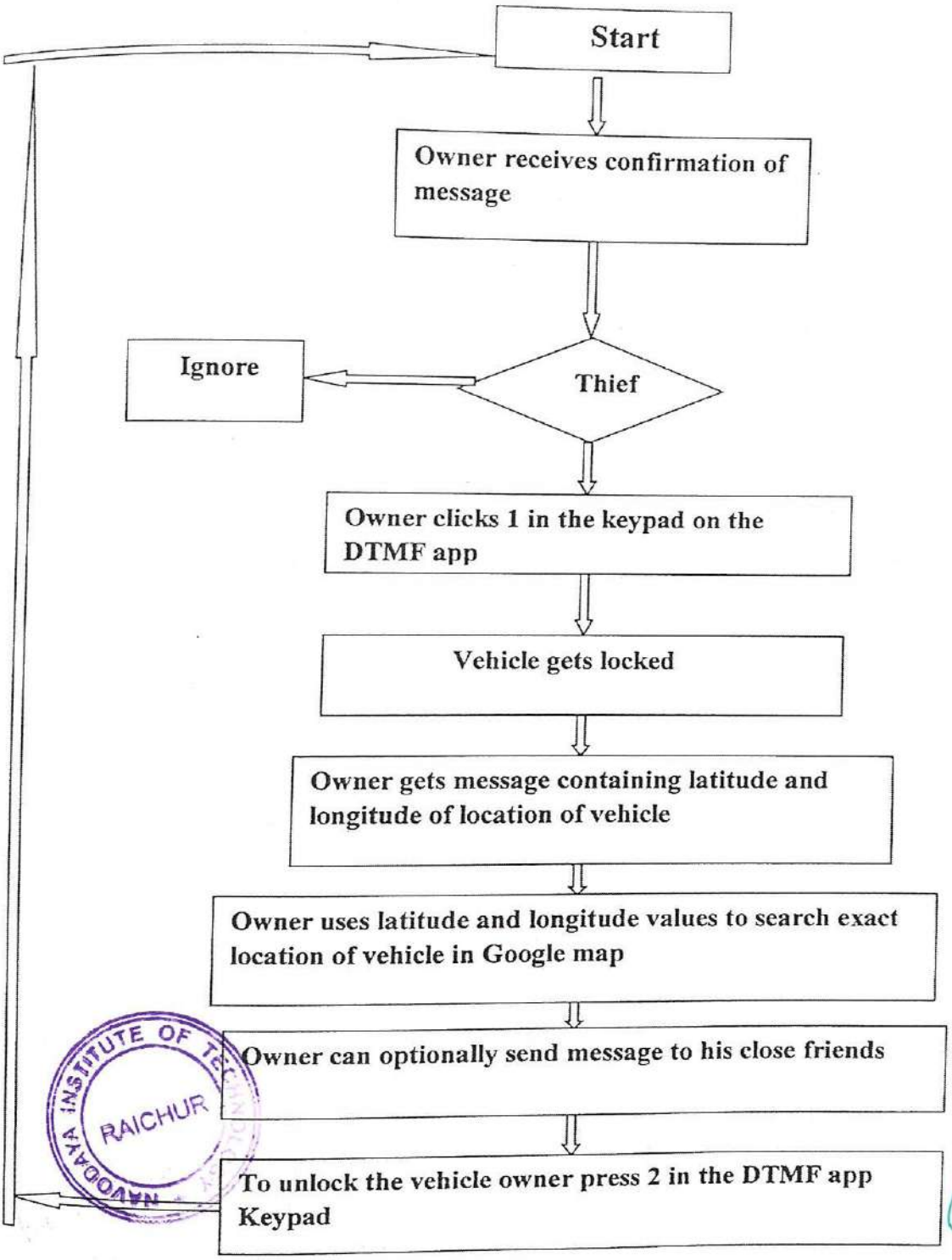


Fig 4.1.1 Use case diagram

4.3 DATA FLOW DIAGRAM

The DFD is also called as bubble chart. It is a simple graphical formalism that can be used to represent a system in terms of input data to the system, various processing carried out on this data, and the output data is generated by this system.



4. ARM processor:

ARM is computer processor based RISC architecture. A RISC-based computer design approach means ARM processors require significantly fewer transistors than typical processors in average computers. This approach reduces costs, heat and power use. The low power consumption of ARM processors has made them very popular.

The ARM architecture (32-bit) is the most widely used architecture in mobile devices, and most popular 32-bit one in embedded systems.

5. Buffers:

Buffers do not affect the logical state of a digital signal (i.e. a logic 1 input results in a logic 1 output whereas logic 0 input results in a logic 0 output). Buffers are normally used to provide extra current drive at the output but can also be used to regularize the logic present at an interface

6. Drivers:

This section is used to drive the relay where the output is complement of input which is applied to the drive but current will be amplified.

7. Relays:

It is an electromagnetic device which is used to drive the load connected across the relay and the o/p of relay can be connected to controller or load for further processing.

8. Buzzer:

A buzzer or beeper is mechanical, electromechanical, or piezoelectric. Typical uses of buzzers and beepers include alarm devices, timers and confirmation of user input such as a mouse click or keystroke.

9. DC motor:

A DC motor relies on the fact that like magnet poles repels and unlike magnetic poles attracts each other. A coil of wire with a current running through it generates an electromagnetic field aligned with the centre of the coil. By switching the current on or off in a coil its magnetic

6.4 CIRCUIT DIAGRAM & EXPLANATION

1. POWER SUPPLY UNIT

The circuit needs two different voltages, +5V & +12V, to work. These dual voltages are supplied by this specially designed power supply.

The power supply, unsung hero of every electronic circuit, plays very important role in smooth running of the connected circuit. The main object of this 'power supply' is, as the name itself implies, to deliver the required amount of stabilized and pure power to the circuit. Every typical power supply contains the following sections:

1. Step-down Transformer: The conventional supply, which is generally available to the user, is 230V AC. It is necessary to step down the mains supply to the desired level. This is achieved by using suitably rated step-down transformer. While designing the power supply, it is necessary to go for little higher rating transformer than the required one. The reason for this is, for proper working of the regulator IC (say KIA 7805) it needs at least 2.5V more than the expected output voltage

2. Rectifier stage: Then the step-downed Alternating Current is converted into Direct Current. This rectification is achieved by using passive components such as diodes. If the power supply is designed for low voltage/current drawing loads/circuits (say +5V), it is sufficient to employ full-wave rectifier with centre-tap transformer as a power source. While choosing the diodes the PIV rating is taken into consideration.

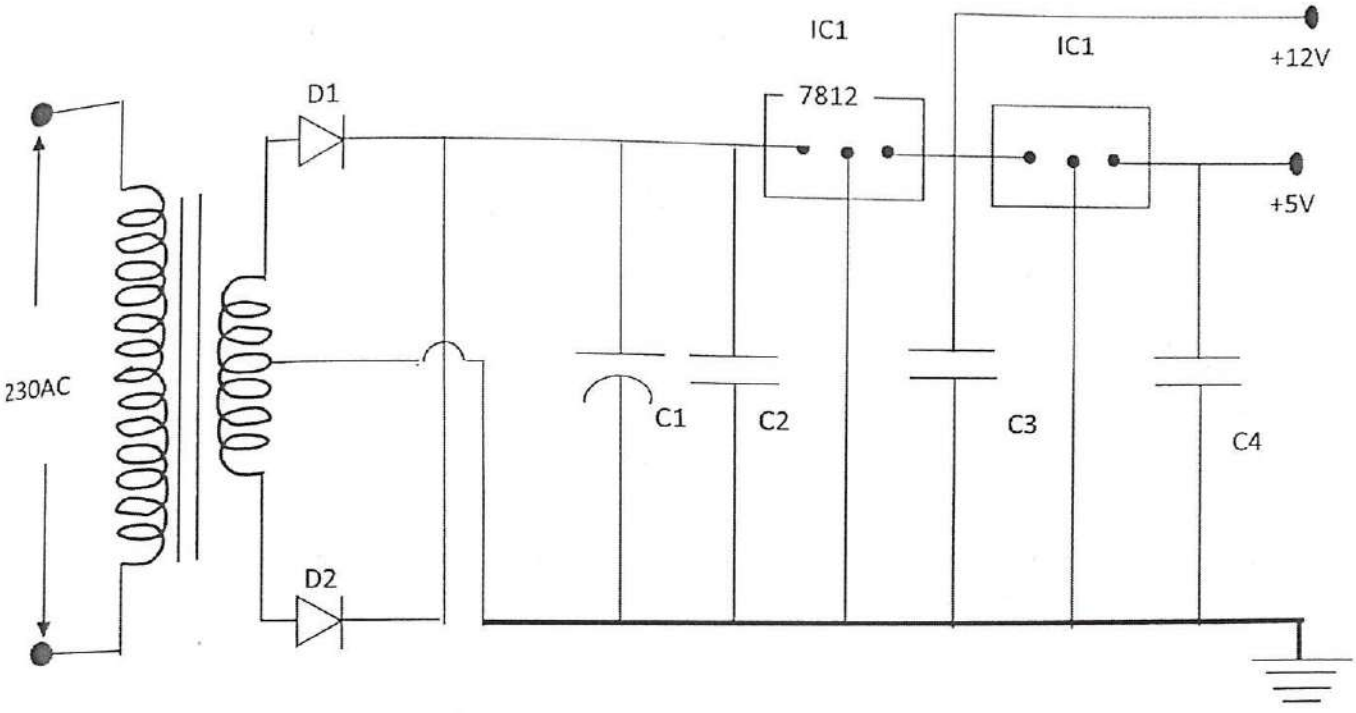
3. Filter stage: But this rectified output contains some percentage of superimposed AC ripples. So to filter these AC components filter stage is built around the rectifier stage. The cheap, reliable, simple and effective filtering for low current drawing loads (say up to 50 mA) is done by using shunt capacitors. This electrolytic capacitor has polarities, take care while connecting the circuit.

4. Voltage Regulation: The filtered DC output is not stable. It varies in accordance with the fluctuations in mains supply or varying load current. This variation of load current is observed due to voltage drop in transformer windings, rectifier and filter circuit. These variations in DC output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. For example, the circuit boards which are implanted by CMOS or TTL ICs.

PRINCIPAL
Navodaya Institute of Technology
RAICHUR-584 103

Head of Department
Computer Science & Engineering
Navodaya Institute of Technology
RAICHUR-584 103

CIRCUIT DIAGRAM OF +5V & +12V FULL WAVE REGULATED POWER



SUPPLY

Fig 6.4.1 Full wave regulated power supply

Parts List:

SEMICONDUCTORS

IC1	7812 Regulator IC	1
IC2	7805 Regulator IC	1
D1& D2	1N4007 Rectifier Diodes	2

CAPACITORS

C1	1000 µf/25V Electrolytic	1
C2 to C4	0.1µF Ceramic Disc type	3

MISCELLANEOUS

X1	230V AC Pri,14-0-14 1Amp Sec Transformer	1

communication between mobile telephones (mobile stations), base stations (cell sites), and switching systems.

Digital Media Formats - GSM is designed to transfer digital information. The initial version of GSM transmitted digital media in **circuit switched** (continuous transmission) form and later versions of GSM deliver data in **packet data** form.

Functional sections: GSM System composed of three key sessions.

1. **Mobile Stations (MS)** - A device that converts media to and from GSM radio signals.
2. **Base Station Subsystem (BSS)** - Assemblies that convert digital signals to radio signals that can be sent to mobile devices and receive radio signals that can be converted back to their digital form. The BSS is divided into **base station - BS** - parts that are located at the cell site and **base station controllers - BSC** - that coordinate the distribution and reception of communication connections
3. **Network and Switching System (NSS)** - The NSS performs the **interconnection** between the **base station** parts and **other networks** such as the public switched telephone network - **PSTN** - and public **Internet**. The NSS is composed of circuit data and packet data switches, databases, and administrative control services.

A GSM network consists of several functional entities, whose functions and interfaces are defined. The GSM network can be divided into following broad parts.

- The Mobile Station (MS)
- The Base Station Subsystem (BSS)
- The Network Switching Subsystem (NSS)
- The Operation Support Subsystem (OSS)

ARCHITECTURAL OVERVIEW:

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro programmed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core. Pipeline techniques are employed so that all parts of the processing and memory system scan operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory. The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue. The key idea behind Thumb is that of a super-reduced instruction set. Essentially, theARM7TDMI-S processor has two instruction sets:

1. The standard 32-bit ARM set.
2. A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same32-bit register set as ARM code. Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bitmemory system. The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30% over Thumb mode.

ON-CHIP FLASH PROGRAM MEMORY:

The LPC2141/42/44/46/48 incorporates a 32kB, 64kB, 128kB, 256kB and 512kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be

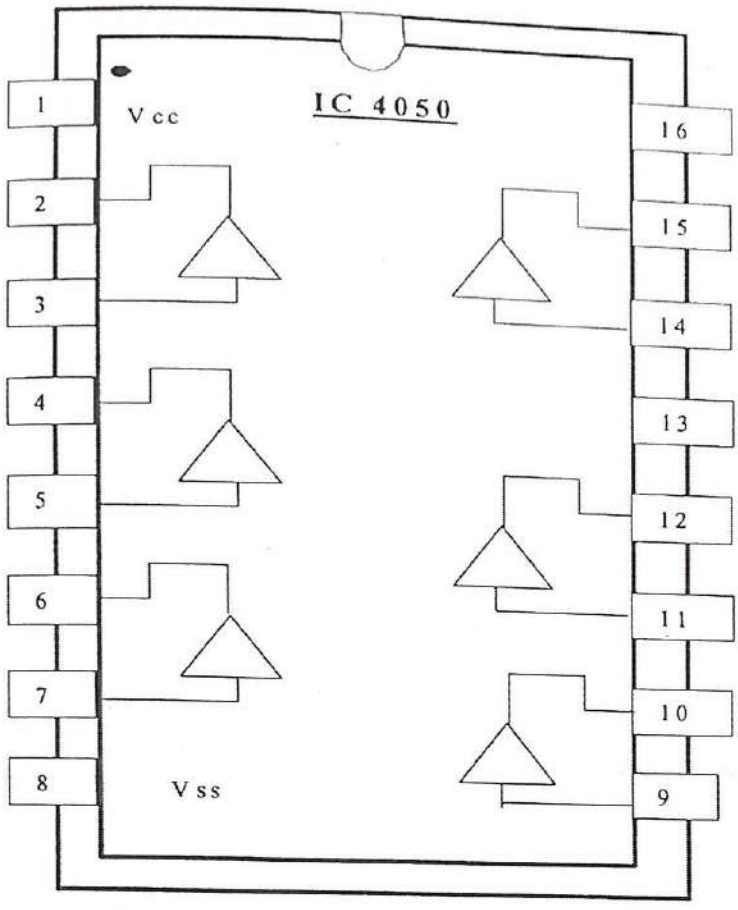


Fig 6.4.6 Hex buffer IC4040

ULN 2003: Since the digital outputs of the some circuits cannot sink much current, they are not capable of driving relays directly. So, high-voltage high-current Darlington arrays are designed for interfacing low-level logic circuitry and multiple peripheral power loads. The series ULN2000A/L ICs drive seven relays with continuous load current ratings to 600mA for each input. At an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously, typical power loads totaling over 260W [400mA x 7, 95V] can be controlled. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. These Darlington arrays are furnished in 16-pin dual in-line plastic packages (suffix A) and 16-lead surface-mountable SOICs (suffix L). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. The input of ULN 2003 is TTL-compatible open-collector outputs. As each of these outputs can sink a maximum collector current of 500 mA, miniature Controller relays can be easily driven. No additional free-wheeling clamp diodes are required to be

Electronics and Communication Engineering

MICROCONTROLLERS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES42	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:
Microprocessors and microcontroller. Introduction, Microprocessors and Microcontrollers, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture, Computer software.
The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization, External Memory interfacing, Stacks.

6 Hours

UNIT 2:
Addressing Modes: Introduction, Instruction syntax, Data types, Subroutines, Addressing modes: Immediate addressing , Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing.
Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction.

6 Hours

UNIT 3:
8051 programming: Assembler directives, Assembly language programs and Time delay calculations.

6 Hours

UNIT 4:
8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming

7 Hours

PART – B

UNIT 5:
8051 Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C .

6 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 19/9/2015
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT 6:

8051 Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C.

8255A Programmable Peripheral Interface:, Architecture of 8255A, I/O addressing,, I/O devices interfacing with 8051 using 8255A.

. 6 Hours

Course Aim – The MSP430 microcontroller is ideally suited for development of low-power embedded systems that must run on batteries for many years. There are also applications where MSP430 microcontroller must operate on energy harvested from the environment. This is possible due to the ultra-low power operation of MSP430 and the fact that it provides a complete system solution including a RISC CPU, flash memory, on-chip data converters and on-chip peripherals.

UNIT 7:

Motivation for MSP430microcontrollers – Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design).

MSP430 RISC CPU architecture, Compiler-friendly features, Instruction set, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families. **2 Hours**

Introduction to Code Composer Studio (CCS v4). Understanding how to use CCS for Assembly, C, Assembly+C projects for · MSP430 microcontrollers. Interrupt programming. **2 Hours**

Digital I/O – I/O ports programming using C and assembly, Understanding the muxing scheme of the MSP430 pins. **3 Hours**

2 Hours

UNIT 8:

On-chip peripherals. Watchdog Timer, Comparator, Op-Amp, Basic Timer, Real Time Clock (RTC), ADC, DAC, SD16, LCD, DMA.

Using the Low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and Interrupt. **2 Hours**

2 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL (18/9/20)
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (N.I.T.)
RAICHUR-584 103

Interfacing LED, LCD, External memory. Seven segment LED modules interfacing. Example – Real-time clock.

2 Hours

Case Studies of applications of MSP430 - Data acquisition system, Wired Sensor network, Wireless sensor network with Chipcon RF interfaces.

3 Hours

TEXT BOOKS:

1. **"The 8051 Microcontroller and Embedded Systems – using assembly and C "-**, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006
2. **"MSP430 Microcontroller Basics"**, John Davies, Elsevier, 2010 (Indian edition available)

REFERENCE BOOKS:

1. **"The 8051 Microcontroller Architecture, Programming & Applications"**, 2e Kenneth J. Ayala ;, Penram International, 1996 / Thomson Learning 2005.
2. **"The 8051 Microcontroller"**, V.Udayashankar and MalikarjunaSwamy, TMH, 2009
3. **MSP430 Teaching CD-ROM,** Texas Instruments, 2008 (can be requested **http://www.unitl.in**)
4. **Microcontrollers: Architecture, Programming, Interfacing and System Design"**,Raj Kamal, "Pearson Education, 2005

CONTROL SYSTEMS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ES43**	**IA Marks**	:	**25**
Hrs/ Week	:	**04**	**Exam Hours**	:	**03**
Total Hrs.	:	**52**	**Exam Marks**	:	**100**

PART – A

UNIT 1:

Modeling of Systems: Introduction to Control Systems, Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical systems, Friction, Translational systems (Mechanical accelerometer, systems excluded), Rotational systems, Gear trains, Electrical systems, Analogous systems.

7 Hours

UNIT 2:

Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded), **6 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT 3:

Time Response of feed back control systems: Standard test signals, Unit step response of First and second order systems, Time response specifications, Time response specifications of second order systems, steady – state errors and error constants. Introduction to PID Controllers(excluding design)

7 Hours

UNIT 4:

Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh- stability criterion, Relative stability analysis; More on the Routh stability criterion.

6 Hours

PART – B

UNIT 5:

Root–Locus Techniques: Introduction, The root locus concepts, Construction of root loci.

6 Hours

UNIT 6:

Frequency domain analysis: Correlation between time and frequency response, Bode plots, Experimental determination of transfer functions, Assessment of relative stability using Bode Plots. Introduction to lead, lag and lead-lag compensating networks (excluding design). **7 Hours**

UNIT 7:

Stability in the frequency domain: Introduction to Polar Plots, (Inverse Polar Plots excluded) Mathematical preliminaries, Nyquist Stability criterion, Assessment of relative stability using Nyquist criterion, (Systems with transportation lag excluded).

7 Hours

UNIT 8:

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations.

6 Hours

TEXT BOOK :

1. **J. Nagarath and M.Gopal,** "Control Systems Engineering", New Age International (P) Limited, Publishers, Fourth edition – 2005.

REFERENCE BOOKS:

1. **"Modern Control Engineering ",** K. Ogata, Pearson Education Asia/ PHI, 4th Edition, 2002.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL 18/9/2017
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

MICROCONTROLLERS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ESL47**	**IA Marks**	:	**25**
Hrs/ Week	:	**03**	**Exam Hours**	:	**03**
Total Hrs.	:	**42**	**Exam Marks**	:	**50**

I. PROGRAMMING

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX .
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter.

Note: Programming exercise is to be done on both 8051 & MSP430.

II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.

8. Simple Calculator using 6 digit seven segment displays and Hex Keyboard interface to 8051.
9. Alphanumeric LCD panel and Hex keypad input interface to 8051.
10. External ADC and Temperature control interface to 8051.
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
12. Stepper and DC motor control interface to 8051.
13. Elevator interface to 8051.

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL 18/9/2012
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers. **7 Hours**

UNIT 7:

Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators. **6 Hours**

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks.

6 Hours

TEXT BOOK:

1. **"Electronic Devices and Circuit Theory"**, Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9TH Edition.

REFERENCE BOOKS:

1. **'Integrated Electronics'**, Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **"Electronic Devices and Circuits"**, David A. Bell, PHI, 4th Edition, 2004
3. **"Analog Electronics Circuits: A Simplified Approach"**, U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	**10ES33**	**IA Marks**	:	**25**
Hrs/ Week	:	**04**	**Exam Hours**	:	**03**
Total Hrs.	:	**52**	**Exam Marks**	:	**100**

PART – A

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables,

INSTITUTE OF TECHNOLOGY ★ NAVO... RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations. **6 Hours**

UNIT 2:
Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables. **7 Hours**

UNIT 3:
Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. **6 Hours**

UNIT 4:
Analysis and design of combinational logic - II: Digital multiplexers-Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics.

7 Hours

PART – B

UNIT 5:
Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The $\overline{S}\,\overline{R}$ Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop. **7 Hours**

UNIT 6:
Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops **7 Hours**

UNIT 7:
Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design.

6 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL 18/9/2021
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT - 8

Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK, frequency hop spread spectrum, applications. **7 Hours**

TEXT BOOK:

1. **Digital communications**, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **Digital and Analog communication systems**, Simon Haykin, John Wildy India Lts, 2008
2. **An introduction to Analog and Digital Communication**, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 2008.
3. **Digital communications** - Bernard Sklar: Pearson education 2007

MICROPROCESSOR

Subject Code	: 10EC62	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

8086 PROCESSORS: Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing. **6 Hours**

UNIT - 2

INSTRUCTION SET OF 8086: Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators. **6 Hours**

UNIT - 3

BYTE AND STRING MANIPULATION: String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display. **7 Hours**

UNIT - 4

8086 INTERRUPTS: 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples. **7 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PART – B

UNIT - 5

8086 INTERFACING: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor. **7 Hours**

UNIT - 6

8086 BASED MULTIPROCESSING SYSTEMS: Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples. **6 Hours**

UNIT - 7

SYSTEM BUS STRUCTURE: Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB) **6 Hours**

UNIT - 8

80386, 80486 AND PENTIUM PROCESSORS: Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor. **7 Hours**

TEXT BOOKS:

1. **Microcomputer systems-The 8086 / 8088** Family – Y.C. Liu and G. A. Gibson, 2E PHI -2003
2. **The Intel Microprocessor, Architecture, Programming and Interfacing**-Barry B. Brey, 6e, Pearson Education / PHI, 2003

REFERENCE BOOKS:

1. **Microprocessor and Interfacing- Programming & Hardware,** Douglas hall, 2nd , TMH, 2006.
2. **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 2nd , 2006.
3. **8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware & Applications** - Triebel and Avtar Singh, 4e, Pearson Education, 2003

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (N.I.T.)
RAICHUR-584 103

TEXT BOOKS:

1. **Antennas and Wave Propagation,** John D. Krauss, 4th Edn,McGraw-Hill International edition, 2010.
2. **Antennas and Wave Propagation** - Harish and Sachidananda: Oxford Press 2007.

REFERENCE BOOKS:

1. **Antenna Theory Analysis and Design** - C A Balanis, 3rd Edn, John Wiley India Pvt. Ltd, 2008.
2. **Antennas and Propagation for Wireless Communication Systems** - Sineon R Saunders, John Wiley, 2003.
3. **Antennas and wave propagation** - G S N Raju: Pearson Education 2005.

OPERATING SYSTEMS

Subject Code	: 10EC65	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS: Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems, distributed operating systems. **6 Hours**

UNIT - 2

STRUCTURE OF THE OPERATING SYSTEMS: Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems. **7 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 18/9/2012
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103.

UNIT - 3

PROCESS MANAGEMENT: Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris. **6 Hours**

UNIT - 4

MEMORY MANAGEMENT: Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program controlled data, kernel memory allocation. **7 Hours**

PART – B

UNIT - 5

VIRTUAL MEMORY: Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory. **6 Hours**

UNIT - 6

FILE SYSTEMS: File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system. **7 Hours**

UNIT - 7

SCHEDULING: Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX. **6 Hours**

UNIT - 8

MESSAGE PASSING: Implementing message passing, Mailboxes, Inter process communication in UNIX. 7 Hours

TEXT BOOK:

1. **"Operating Systems - A Concept based Approach"**, D. M. Dhamdhare, TMH, 3rd Ed, 2010.

REFERENCE BOOK:

1. **Operating Systems Concepts**, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th Edition, 2001.
2. **Operating System – Internals and Design Systems**, Willaim Stalling, Pearson Education, 4th Ed, 2006.
3. **Design of Operating Systems**, Tennambhaum, TMH, 2001.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL 18/9/2021
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ADVANCED COMMUNICATION LAB

Subject Code	: 10ECL67	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs.: 42		Exam Marks	: 50

LIST OF EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW – 2009 can be used for verification and testing.

1. TDM of two band limited signals.
2. ASK and FSK generation and detection
3. PSK generation and detection
4. DPSK generation and detection
5. QPSK generation and detection
6. PCM generation and detection using a CODEC Chip
7. Measurement of losses in a given optical fiber (propagation loss, bending loss) and numerical aperture
8. Analog and Digital (with TDM) communication link using optical fiber.
9. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench
10. Measurement of directivity and gain of antennas: Standard dipole (or printed dipole), microstrip patch antenna and Yagi antenna (printed).
11. Determination of coupling and isolation characteristics of a stripline (or microstrip) directional coupler
12. (a) Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant of the substrate. (b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

MICROPROCESSOR LAB

Subject Code	: 10ECL68	IA Marks	: 25
No. of Practical Hrs/Week: 03		Exam Hours	: 03
Total no. of Practical Hrs.: 42		Exam Marks	: 50

I) Programs involving

1) Data transfer instructions like:
   i] Byte and word data transfer in different addressing modes.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL 18/9/2022.
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ii] Block move (with and without overlap)
iii] Block interchange

2) Arithmetic & logical operations like:
   i] Addition and Subtraction of multi precision nos.
   ii] Multiplication and Division of signed and unsigned Hexadecimal nos.
   iii] ASCII adjustment instructions
   iv] Code conversions
   v] Arithmetic programs to find square cube, LCM, GCD, factorial

3) Bit manipulation instructions like checking:
   i] Whether given data is positive or negative
   ii] Whether given data is odd or even
   iii] Logical 1's and 0's in a given data
   iv] 2 out 5 code
   v] Bit wise and nibble wise palindrome

4) Branch/Loop instructions like:
   i] Arrays: addition/subtraction of N nos.
   Finding largest and smallest nos.
   Ascending and descending order
   ii] Near and Far Conditional and Unconditional jumps, Calls and Returns

5) Programs on String manipulation like string transfer, string reversing, searching for a string, etc.

6) Programs involving Software interrupts
   Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console

II) Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output-PCI bus compatible) card
   a) Matrix keyboard interfacing
   b) Seven segment display interface
   c) Logical controller interface
   d) Stepper motor interface

III) Other Interfacing Programs
   a) Interfacing a printer to an X86 microcomputer
   b) PC to PC Communication

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT - 7

DC CHOPPERS: Introduction, Principles of step down and step up choppers, Step down chopper with RL loads, Chopper classification, Switch mode regulators – buck, boost and buck – boost regulators. **6 Hours**

UNIT - 8

INVERTORS: Introduction, Principles of operation, Performance parameters, 1φ bridge inverter, voltage control of 1φ invertors, current source invertors, Variable DC link inverter.

7 Hours

TEXT BOOKS:

1. **"Power Electronics"** - M. H. Rashid 3rd edition, PHI / Pearson publisher 2004.
2. **"Power Electronics"** - M. D. Singh and Kanchandani K.B. TMH publisher, 2nd Ed. 2007.

REFERENCE BOOKS:

1. **"Power Electronics, Essentials and Applications", L Umanand,** John Wiley India Pvt. Ltd, 2009.
2. **"Power Electronics"** , Daniel W. Hart, McGraw Hill, 2010.
3. **"Power Electronics"**, V Nattarasu and R.S. Anandamurhty, **Pearson/Sanguine Pub. 2006.**

EMBEDED SYSTEM DESIGN

Subject Code	: **10EC74**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT 1:

Introduction to Embedded System: Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process. **5 Hours**

UNIT 2:

The Hardware Side: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL 16/9/17
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour)
The concepts of State and Time, The State Diagram, Finite State Machines-A Theoretical Model.

8 Hours

UNIT 3:
Memories and the Memory Subsystem: Classifying Memory, A General Memory Interface, ROM Overview, Static RAM Overview, Dynamic RAM Overview, Chip Organization, Terminology, A Memory Interface in Detail, SRAM Design, DRAM Design, DRAM Memory Interface, The Memory Map, Memory Subsystem Architecture, Basic Concepts of Caching, Designing a Cache System, Dynamic Memory Allocation.

7 Hours

UNIT 4:
Embedded Systems Design and Development : System Design and Development, Life-cycle Models, Problem Solving-Five Steps to Design, The Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project.

6 Hours

PART – B

UNIT 5 & 6:
Real-Time Kernels and Operating Systems: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited.

12 Hours

UNIT 7 & 8:
Performance Analysis and Optimization: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance.

12 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

REAL-TIME SYSTEMS

Subject Code	: 10EC762	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1
INTRODUCTION TO REAL-TIME SYSTEMS: Historical background, RTS Definition, Classification of Real-time Systems, Time constraints, Classification of Programs. **6 Hours**

UNIT - 2
CONCEPTS OF COMPUTER CONTROL: Introduction, Sequence Control, Loop control, Supervisory control, Centralised computer control, Distributed system, Human-computer interface, Benefits of computer control systems. **6 Hours**

UNIT - 3
COMPUTER HARDWARE REQUIREMENTS FOR RTS: Introduction, General purpose computer, Single chip microcontroller, Specialized processors, Process-related Interfaces, Data transfer techniques, Communications, Standard Interface. **7 Hours**

UNIT - 4
LANGUAGES FOR REAL-TIME APPLICATIONS: Introduction, Syntax layout and readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation, Data types, Control Structure, Exception Handling, Low-level facilities, Co routines, Interrupts and Device handling, Concurrency, Real-time support, Overview of real-time languages. **7 Hours**

PART – B

UNIT - 5 & 6
OPERATING SYSTEMS: Introduction, Real-time multi-tasking OS, Scheduling strategies, Priority Structures, Task management, Scheduler and real-time clock interrupt handles, Memory Management, Code sharing, Resource control, Task co-operation and communication, Mutual exclusion, Data transfer, Liveness, Minimum OS kernel, Examples. **14 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT - 7

DESIGN OF RTSS – GENERAL INTRODUCTION: Introduction, Specification documentation, Preliminary design, Single-program approach, Foreground/background, Multi-tasking approach, Mutual exclusion, Monitors. **6 Hours**

UNIT - 8

RTS DEVELOPMENT METHODOLOGIES: Introduction, Yourdon Methodology, Requirement definition for Drying Oven, Ward and Mellor Method, Hately and Pirbhai Method. **6 Hours**

TEXT BOOKS:

1. **Real - Time Computer Control- An Introduction**, Stuart Bennet, 2nd Edn. Pearson Education. 2005.

REFERENCE BOOKS:

1. **Real-Time Systems Design and Analysis**, Phillip. A. Laplante, second edition, PHI, 2005.
2. **Real-Time Systems Development**, Rob Williams, Elsevier. 2006.
3. **Embedded Systems**, Raj Kamal, Tata Mc Graw Hill, India, 2005.

IMAGE PROCESSING

Subject Code	: **10EC763**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

DIGITAL IMAGE FUNDAMENTALS: What is Digital Image Processing. fundamental Steps in Digital Image Processing, Components of an Image processing system, elements of Visual Perception. **6 Hours**

UNIT - 2

Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships between Pixels, Linear and Nonlinear Operations. **6 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103.

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

VIII SEMESTER
WIRELESS COMMUNICATION

Subject Code	: 10EC81	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

Introduction to wireless telecommunication systems and Networks, History and Evolution Different generations of wireless cellular networks 1G, 2g,3G and 4G networks. **6 Hours**

UNIT - 2

Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components, Cellular component identification Call establishment. **7 Hours**

UNIT - 3

Wireless network architecture and operation, Cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backbone networks, Mobility management, Radio resources and power management Wireless network security. **7 Hours**

UNIT - 4

GSM and TDMA techniques, GSM system overview, GSM Network and system Architecture, GSM channel concepts, GSM identifiers **6 Hours**

PART – B

UNIT - 5

GSM system operation, Traffic cases, Cal handoff, Roaming, GSM protocol architecture. TDMA systems. **6 Hours**

UNIT - 6

CDMA technology, CDMA overview, CDMA channel concept CDMA operations. **6 Hours**

UNIT - 7

Wireless Modulation techniques and Hardware, Characteristics of air interface, Path loss models, wireless coding techniques, Digital modulation

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103.

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

techniques, OFDM, UWB radio techniques, Diversity techniques, Typical GSM Hardware.

7 Hours

UNIT - 8

Introduction to wireless LAN 802.11X technologies, Evolution of Wireless LAN Introduction to 802.15X technologies in PAN Application and architecture Bluetooth Introduction to Broadband wireless MAN, 802.16X technologies.

7 Hours

TEXT BOOK:

1. **Wireless Telecom Systems and networks,** Mullet: Thomson Learning 2006.

REFERENCE BOOKS:

1. **Mobile Cellular Telecommunication,** Lee W.C.Y, MGH, 2nd, 2009.
2. **Wireless communication** - D P Agrawal: 2nd Edition Thomson learning 2007.
3. **Fundamentals of Wireless Communication,** David Tse, Pramod Viswanath, Cambridge 2005.
4. S, S. Manvi, M. S. Kakkasageri, **"Wireles and Mobile Network concepts and protocols"**, John Wiley India Pvt. Ltd, 1st edition, 2010.
5. **"Wireless Communication – Principles & Practice"** , T.S. Rappaport, PHI 2001.

DIGITAL SWITCHING SYSTEMS

Subject Code	: **10EC82**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

Developments of telecommunications, Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH, Transmission performance.

7 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103.

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

18/9/2021

REALTIME OPERATING SYSTEMS

Subject Code	: 10EC842	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT 1

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. **6 Hours**

UNIT 2

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions. **7 Hours**

UNIT 3

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. **6 Hours**

UNIT 4

I/O Resources:

Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory:

Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems. **7 Hours**

PART – B

UNIT 5

Multiresource Services:

Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:

Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. **7 Hours**

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT 6

Embedded System Components:
Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:
Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.
7 Hours

UNIT 7

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations. **6 Hours**

UNIT 8

High availability and Reliability Design:
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. (Chap 13 of book Myke Predko)
7 Hours

REFERENCE BOOKS:

1. **"Real-Time Embedded Systems and Components"** Sam Siewert, Cengage Learning India Edition, 2007.
2. **" Programming and Customizing the PIC microcontroller" ,** Myke Predko, 3rd Ed, TMH, 2008

GSM

Subject Code	: **10EC843**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART – A

UNIT - 1

GSM ARCHITECTURE AND INTERFACES: Introduction, GSM frequency bands, GSM PLMN, Objectives of a GSM PLMN, GSM PLMN Services, GSM Subsystems, GSM Subsystems entities, GSM interfaces, The radio interface (MS to BSC), A_{bits} interface (BTS to BSC), A interface (BSC

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 18/5/11
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology
RAICHUR-584 103

NAVODAYA
RAICHUR

NAVODAYA INSTITUTE OF TECHNOLOGY
BIJJANAGERA ROAD, RAICHUR-584103
(Affiliation to Visvesvaraiya Technological University, Belgaum)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the project work entitled **"HEAD CONTROLLED MOUSE"** carried out by **Mr.DEEPAK A(USN:3NA12EC008), Mr.SHAIK MAHEBOOB PEERA (USN: 3NA12EC017), Mr.SHARANABASAVA GOOGAL(USN:3NA12EC018), Ms. POOJA PK (USN: 3NA12EC014)** is a bonafide student of **NAVODAYA INSTITUTE OF TECHNOLOGY, RAICHUR** in partial fulfillment for the award of **Bachelor of Engineering**in Electronics And Communication Engineeringof the Visvesvaraiya Technological University, Belgaum, during the year **2015-2016.**It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Guide	HOD	Principal
02/06/2016	11/6/2016	
Prof. Laxmikant Reddi	**Dr. K M PALANISWAMY**	**Dr. Shivaprakash.C.K**

External Viva

Name of the examiners	Signature with date
1. S. Ramanjaneya	
2. Prof Mahesh.V	

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ABSTRACT

Easy Input is a head-controlled keyboard and mouse input device for paralyzed users. This study describes the motivation and the design considerations of an economical head-operated computer mouse. In addition it focuses on the invention of a head-operated computer mouse that employs tilt sensors placed in the headset to determine head position and to function as simple head operated computer mouse. One tilt sensor detects the lateral head motion to drive the left or right displacement of the mouse.

The system uses accelerometers to detect the user's head tilt in order to direct mouse movement on the monitor. The clicking of the mouse is activated by the user's eye blinking through a sensor. The keyboard function is implemented by allowing the user to scroll through letters with head tilt and with eye blinking as the selection mechanism.

We constructed an interface system that would allow a sin-Wady paralyzed user to interact with a computer with almost full functional capability. That is, the system operates as a mouse initially, but the user has the ability to toggle in and out of a keyboard mode allowing the entry of text. This is achieved by using the control from a single eye, tracking the position of the pupil for direction, and using blinking as an input. As detection of eye motion proved too challenging, we built an accelerometer based tilt detector to determine head motion, so that, although not as applicable in this particular case, it might be use by a quadriplegic individual.

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CONTENT:

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER-1

INTRODUCTION

Although a wealth of software exists, severely disabled people cannot benefit from it because of difficulties of access, which is usually via computer keyboard or mouse. A Computer Control System has been developed which enables this software to be utilized. In the case described. Computer control system is a computer input device for physically disabled and paralyzed users.

The system uses accelerometer to detect the users head tilt in order to direct mouse movement on the monitor. The keyboard function is implemented by allowing the user to scroll through letters with head tilt and with eye blink sensor as the selection mechanism.

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER-3

OVERALL CONCEPT

We constructed an interface system that would allow a similarly paralyzed user to interact with a computer with almost full functional capability. That is, the system operates as a mouse initially, but the user has the ability to type using an onscreen virtual keyboard allowing the entry of text. We built an accelerometer based tilt detector to determine head motion, so that, although not as applicable in this particular case, it this particular case, it might be used by a quadriplegic individual.

Working Concept:

- The system uses 3-axis accelerometer to detect the user's head tilt in X-Y axis to direct mouse movement on the monitor.
- The clicking of the mouse is activated by user's eye blinking through a eye blink sensor.
- The keyboard function is implemented by allowing the user to select letters using onscreen virtual keyboard with head tilt.

Course Work Required:

- **Microchip, P89V51 Microcontroller**-Features, Pin configurations, programming commands, system clock and clock options, Interrupts, I/O ports, external interrupts, IC Serial Peripheral Interface, Data Sheet.
- **Free scale 3g, 3-Axis Accelerometer-** features, maximum ratings, operating characteristics, principle of operation, basic connections.
- **Eye Blink sensorusing** IR sensor and comparator.
- **Receiver-RS-232** serial port, features, pin out diagram, operating characteristics.
- **.NET Development kit-** Basic program designing, serial communication commands and its dependencies, commands, compiling, debugging, file generations.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL 18/5/2016
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

3.1 Technical Specifications:

1) Microchip P89V51RD2FN

- 80C51 CPU
- 5 V operating voltage from 0 MHz to 40 MHz
- 16/32/64 KB of on-chip flash user code memory with ISP and IAP
- Supports 12-clock (default) or 6-clock mode selection via software or ISP
- Four 8-bit I/O ports with three high-current port 1 pins (16 mA each)
- Three 16-bit timers/counters
- Programmable watchdog timer
- TTL- and CMOS-compatible logic levels

2) ADXL335 Three-Axis Acceleration Sensor

- 3-axis sensing
- Low power : 350 µA (typical)
- Single-supply operation: 1.8 V to 3.6 V
- Excellent temperature stability
- BW adjustment with a single capacitor per axis
- Integral Signal Conditioning with low pass filter.

3) Regulators

- 3-terminal Positive Regulator
- Output voltages of 3v & 5v
- Adjustable Output Regulator.

4) Eye Blink Sensor

- Voltage 0 to 5v
- Output Current 75mA
- Adjustment: Potentiometer
- Blinking of eye is exactly using comparators.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 18/9/2024
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER-4

BLOCK DIAGRAM DESCRIPTION

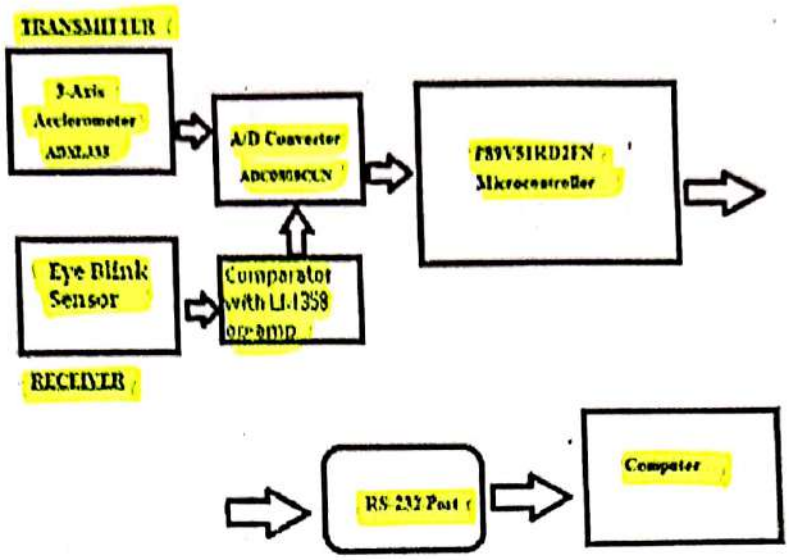


Fig 4.0

We use 3-axis accelerometer (ADXL335) to detect the head movement in X-Y direction and a Eye blink Sensor for detecting Click.

Accelerometer sensor outputs are connected to an A/D converter channels on the microcontroller. And Eye Blink sensor is connected to ADC which acts as a right of the mouse. Processed digital information's transmitted through an 89V51 microcontroller USART pins.

On the other hand, a RS-232 receiver collects all the correct information and processes this information by serial communication driver written in .NET and then the computer process this information and this hardware interfaced will work as a mouse.

A RS-232 software driver acts as an intermediate between the RS-232 serial hardware and computer, to support the sensor signal and process the information as per program.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 18/5/2016
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Electronics & Communication Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Electrical and Electronics Engineering

10EE61 POWER SYSTEM ANALYSIS AND STABILITY

Subject Code	:	10EE61	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART - A

UNIT - 1

REPRESENTATION OF POWER SYSTEM COMPONENTS: Circuit models of Transmission line, Synchronous machines, Transformers and load. Single line diagram, impedance and reactance diagrams. Per unit system, per unit impedance diagram of power system. 8 Hours

UNIT - 2

SYMMETRICAL 3 - PHASE FAULTS: Analysis of Synchronous machines and Power system Transients on a transmission line, Short-Circuit currents and the reactance of synchronous machines with and without load. 6 Hours

UNIT - 3 & 4

SYMMETRICAL COMPONENTS: Introduction, analysis of unbalanced load against balanced Three-phase supply, neutral shift. Resolution of unbalanced phasors into their symmetrical components. Phase shift of symmetrical components in star-delta transformer bank, Power in terms of symmetrical components, Analysis of balanced and unbalanced loads against unbalanced 3 phase supply. Sequence impedances and networks of power system elements (alternator, transformer and transmission line) Sequence networks of power systems. Measurement of sequence impedance of synchronous generator. 12 Hours

Part - B

UNIT - 5 & 6

UNSYMMETRICAL FAULTS: L-G, L-L, L-L-G faults on an unbalanced alternator with and without fault impedance. Unsymmetrical faults on a power system with and without fault impedance. Open conductor faults in power system. 14 Hours

UNIT - 7

STABILITY STUDIES: Introduction, Steady state and transient stability. Rotor dynamics and the swing equation. Equal area criterion for transient stability evaluation and its applications. 8 Hours

UNIT – 8

UNBALANCED OPERATION OF THREE PHASE INDUCTION MOTRORS: Analysis of three phase induction motor with one line open., Analysis of three phase induction motor with unbalanced voltage. 4 Hours

TEXT BOOKS:

1. Elements of Power System Analysis, W.D.Stevenson, TMH,4th Edition
2. Modern Power System Analysis, I. J. Nagrath and D.P.Kothari - TMH, 3rd Edition,2003.
3. Symmetrical Components and Short Circuit Studies, Dr.P.N.Reddy, Khanna Publishers

REFERENCE BOOKS:

1. Power System Analysis, Hadi Sadat, TMH,2nd Edition.
2. Power system Analysis, R.Bergen, and Vijay Vittal, Pearson Publications, 2nd edition, 2006.

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL 18/9/2014
Navodaya Institute of Technology (R&D)
RAICHUR-584 103

MICROCONTROLLERS

(Common to EC/TC/EE/IT BM/ML)

Sub Code	:	10ES42	*IA Marks*	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Microprocessors and microcontroller: Introduction, Microprocessors and Microcontrollers, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture, Computer software.

The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization, External Memory interfacing, Stacks.

6 Hours

UNIT 2:

Addressing Modes: Introduction, Instruction syntax, Data types, Subroutines, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing.

Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instructions.

5 Hours

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL 16/9/2021
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT 3:

8051 programming: Assembler directives, Assembly language programs and Time delay calculations.

6 Hours

UNIT 4:

8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming

7 Hours

UNIT 5:

8051 Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C.

6 Hours

UNIT 6:

8051 Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C.

8255A Programmable Peripheral Interface: Architecture of 8255A, I/O addressing, I/O devices interfacing with 8051 using 8255A.

6 Hours

Course Aim – The MSP430 microcontroller is ideally suited for development of low-power embedded systems that must run on batteries for many years. There are also applications where MSP430 microcontroller must operate on energy harvested from the environment. This is possible due to the ultra-low power operation of MSP430 and the fact that it provides a complete system solution including a RISC CPU, flash memory, on-chip data converters and on-chip peripherals.

UNIT 7:

Motivation for MSP430microcontrollers – Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design).

2 Hours

MSP430 RISC CPU architecture, Compiler-friendly features, Instruction set, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families.

2 Hours

Introduction to Code Composer Studio (CCS v4). Understanding how to use CCS for Assembly, C, Assembly–C projects for MSP430 microcontrollers. Interrupt programming.

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY ★ RAICHUR

PRINCIPAL 18/9/2020
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

10EE45 POWER ELECTRONICS

Subject Code	:	10EE45	IA Marks	:	25
No. of Lecture Hrs / Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:

Power Semiconductor Devices:
Introduction to semiconductors, Power Electronics, Power semiconductor devices, Control Characteristics. Types of power electronic converters and industrial applications-Drives, Electrolysis, Heating, Welding, Static Compensators, SMPS, HVDC power transmission, Thyristorized tap changers and Circuit breakers.
7 hours

UNIT 2:

Power Transistors: Power BJT's – switching characteristics, switching limits, base drive control. Power MOSFET's and IGBT's –characteristics, gate drive, di/dt and dv/dt limitations. Isolation of gate and base drives. Simple design of gate and base drives.
6 Hours

UNIT 3:

Thyristors
Introduction, Two Transistor Model, characteristics-static and dynamic. di/dt and dv/dt protection. Ratings of thyristors. Thyristor types. Series and parallel operation of Thyristors. Thyristor firing circuits. Design of firing circuits using UJT, R,-R-C circuits. Analysis of firing circuits using operational amplifiers and digital IC's.
7 Hours

UNIT 4:

Commutation Techniques: Introduction. Natural Commutation. Forced commutation- self-commutation, impulse commutation, resonant pulse commutation and complementary commutation.
6 Hours

PART – B

UNIT 5:

Controlled Rectifiers: Introduction. Principle of phase controlled converter operation. Single- phase semi-converters. Full converters. Three-phase half-wave converters. Three-phase full-wave converters.
7.Hours

UNIT 6:

Choppers: Introduction. Principle of step-down and step-up chopper with R-L load. Performance parameters. Chopper classification. Analysis of impulse commutated thyristor chopper (only qualitative analysis) 6 Hours

UNIT 7:

Inverters: Introduction. Principle of operation. Performance parameters. Single-phase bridge inverters. Threephase inverters. Voltage control of single-phase inverters – single pulse width, multiple pulse width, and sinusoidal pulse width modulation. Current source inverters.
7 Hours

UNIT 8:

(a).AC Voltage Controllers: Introduction. Principle of ON-OFF and phase control. Single-phase, bi-directional controllers with resistive and R-L loads.
(b) Electromagnetic Compatibility: Introduction, effect of power electronic converters and remedial measures.

6 Hours

Text Book:

1. Power Electronics, M.H.Rashid, , Pearson, 3rd Edition, 2006.

2. Power Electronics, M.D. Singh and Khanchandani K.B., T.M.H., 2nd Edition,2001

Reference:

1. Power Electronics Essentials and Applications,L.Umanand, Wiley India Pvt Ltd,Reprint,2010
2. Thyristorised Power Controllers, G.K. Dubey, S.R. Doradla, A. Joshi and R.M.K. Sinha, New Age International Publishers.
3. Power Electronics – Converters, Applications and Design, Ned Mohan, Tore M. Undeland, and William P. Robbins, Third Edition, John Wiley and Sons, 2008.
4. Power Electronics: A Simplified Approach, R.S. Ananda Murthy and V. Nattarasu, pearson/Sanguine Technical Publishers.

10EE61 POWER SYSTEM ANALYSIS AND STABILITY

Subject Code	:	10EE61	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART - A

UNIT - 1

REPRESENTATION OF POWER SYSTEM COMPONENTS: Circuit models of Transmission line, Synchronous machines, Transformers and load. Single line diagram, impedance and reactance diagrams. Per unit system, per unit impedance diagram of power system. 8 Hours

UNIT - 2

SYMMETRICAL 3 - PHASE FAULTS: Analysis of Synchronous machines and Power system. Transients on a transmission line, Short-Circuit currents and the reactance of synchronous machines with and without load. 6 Hours

UNIT - 3 & 4

SYMMETRICAL COMPONENTS: Introduction, analysis of unbalanced load against balanced Three-phase supply, neutral shift. Resolution of unbalanced phasors into their symmetrical components. Phase shift of symmetrical components in star-delta transformer bank. Power in terms of symmetrical components, Analysis of balanced and unbalanced loads against unbalanced 3 phase supply. Sequence impedances and networks of power system elements (alternator, transformer and transmission line) Sequence networks of power systems. Measurement of sequence impedance of synchronous generator. 12 Hours

Part - B

UNIT - 5 & 6

UNSYMMETRICAL FAULTS: L-G, L-L, L-L-G faults on an unbalanced alternator with and without fault impedance. Unsymmetrical faults on a power system, with and without fault impedance. Open conductor faults in power system. 14 Hours

UNIT - 7

STABILITY STUDIES: Introduction, Steady state and transient stability, Rotor dynamics and the swing equation. Equal area criterion for transient stability evaluation and its applications. 8 Hours

UNIT – 8

UNBALANCED OPERATION OF THREE PHASE INDUCTION MOTRORS: Analysis of three phase induction motor with one line open., Analysis of three phase induction motor with unbalanced voltage. 4 Hours

TEXT BOOKS:

1. Elements of Power System Analysis, W.D.Stevenson, TMH, 4th Edition
2. Modern Power System Analysis, I. J. Nagrath and D.P.Kothari- TMH, 3rd Edition,2003.
3. Symmetrical Components and Short Circuit Studies, Dr.P.N.Reddy, Khanna Publishers

REFERENCE BOOKS:

1. Power System Analysis, Hadi Sadat, TMH, 2nd Edition
2. Power system Analysis, R.Bergen, and Vijay Vittal, Pearson publications, 2nd edition, 2006.

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

18/9/2012

10EE62 SWITCHGEAR & PROTECTION

Subject Code	:	10EE62	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs	:	52	Exam Marks	:	100

PART - A

UNIT - 1

SWITCHES AND FUSES: Introduction, energy management of power system, definition of switchgear, switches - isolating, load breaking and earthing. Introduction to fuse, fuse law, cut -off characteristics,: Time current characteristics, fuse material, HRC fuse, liquid fuse, Application of fuse

4 Hours

UNIT - 2

PRINCIPLES OF CIRCUIT BREAKERS: Introduction, requirement of a circuit breakers, difference between an isolator and circuit breaker, basic principle of operation of a circuit breaker, phenomena of arc, properties of arc, initiation and maintenance of arc, arc interruption theories - slepian's theory and energy balance theory, Restriking voltage, recovery voltage, Rate of rise of Restriking voltage, DC circuit breaking, AC circuit breaking, current chopping, capacitance switching, resistance switching, Rating of Circuit breakers.

10 Hours

UNIT - 3 & 4

CIRCUITS BREAKERS: Air Circuit breakers – Air break and Air blast Circuit breakers, oil Circuit breakers - Single break, double break, minimum OCB, SF_6 breaker - Preparation of SF_6 gas, Puffer and non Puffer type of SF_6 breakers. Vacuum circuit breakers - principle of operation and constructional details. Advantages and disadvantages of different types of Circuit breakers, Testing of Circuit breakers, Unit testing, synthetic testing, substitution test, compensation test and capacitance test.

LIGHTNING ARRESTERS: Causes of over voltages – internal and external, lightning, working principle of different types of lightning arresters. Shield wires.

12 Hours

PART - B

UNIT - 5

PROTECTIVE RELAYING: Requirement of Protective Relaying. Zones of protection, primary and backup protection. Essential qualities of Protective Relaying. Classification of Protective Relays

4 Hours

UNIT - 6

INDUCTION TYPE RELAY: Non-directional and directional over current relays, IDMT and Directional characteristics. Differential relay – Principle of operation, percentage differential relay, bias characteristics, distance relay – Three stepped distance protection, Impedance relay, Reactance relay, Mho relay, Buchholz relay. Negative Sequence relay, Microprocessor based over current relay – block diagram approach.

10 Hours

UNIT - 7 & 8

PROTECTION SCHEMES: Generator Protection - Merz price protection, prime mover faults, stator and rotor faults, protection against abnormal conditions – unbalanced loading, loss of excitation, over speeding. Transformer Protection - Differential protection, differential relay with harmonic restraint. Inter turn faults Induction motor protection - protection against electrical faults such as phase fault, ground fault, and abnormal operating conditions such as single phasing, phase reversal, over load.

12 Hours

TEXT BOOKS:,

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL 16/9/2013
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

1. Switchgear & Protection Sunil S Rao, Khanna Publishers, 13th Edition, 2008.
2. Power System Protection & Switchgear, Badriram & Viswa Kharma, TMH, 1st edition, 2001.
3. Fundamentals of Power System protection, Y G. Paithankar and S R. Bhide, PHI, 2009.

REFERENCE BOOKS:

1. A Course in Electrical Power, Soni, Gupta & Bhatnagar, Dhanapatrai.
2. Power System Protection & Switchgear, Ravindarnath & Chandra -New age Publications.
3. Electrical Power, Dr S. L. Uppal, Khanna Publishers.
4. Handbook of Switchgears, BHEL, TMH, 5th reprint, 2008.

10EE662 ADVANCED POWER ELECTRONICS

Subject Code	:	10EE662	IA Marks	:	25
No. of Lecture Hrs/ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART - A

UNIT - 1 & 2

DC-DC SWITCHED MODE CONVERTERS: Topologies. Buck, boost, buck-boost, and Cuk converters. Full Bridge DC-DC converter-detailed theory, working principles, modes of operation, with detailed circuits and wave forms, applications, merits and demerits. 16 Hours

UNIT - 3 & 4

DC-AC SWITCHED MODE INVERTERS: Single-phase inverters, three phase inverters. SPWM inverter, detailed theory, working principles, modes of operation with circuit analysis, applications, merits and demerits, problems based on input output voltage relationship.

10 Hours

PART - B

UNIT - 5

RESONANT CONVERTERS: Zero voltage and zero current switching, resonant switch converters, and comparison with hard switching, switching locus diagrams, and working principle. 8 Hours

UNIT - 6

HIGH FREQUENCY INDUCTOR AND TRANSFORMERS: Design principles, definitions, comparison with conventional design and problems. Design of Flyback transformer. 08 Hours

UNIT - 7 & 8

POWER SUPPLIES: Introduction, DC power supplies: fly back converter, forward converter, push-pull converter, half bridge converter, full bridge converter, AC power supplies: switched mode ac power supplies, resonant ac power supplies, bidirectional ac power supplies. 10 Hours

TEXT BOOKS:

1. Power Electronics, Daniel W Hart, TMH, First Edition, 2010.
2. Power Electronics - converters, application & design, Mohan N, Undeland T.M., Robins, W.P John Wiley 3rd Edition 2008
3. Power Electronics-Circuits, Devices, applications, Rashid M H., PHI, 3rd Edition, 2008.

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

10EES2 POWER SYSTEM OPERATION AND CONTROL

Subject Code	:	10EES2	IA Marks	:	25
No. of Lecture Hrs / Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART - A

UNIT - 1

CONTROL CENTER OPERATION OF POWER SYSTEMS:

Power system control and operating states, control center, digital computer configuration, automatic generation control, area control error, operation without central computers, expression for tie-line flow and frequency deviation, parallel operation of generators, area lumped dynamic model. 8 Hours

UNIT - 2 & 3

AUTOMATIC VOLTAGE REGULATOR: Basic generator control loops, Cross-coupling between control loops, Exciter types, Exciter modeling, Generator modeling, Static performance of AVR loop.

AUTOMATIC LOAD FREQUENCY CONTROL:

Automatic Load frequency control of single area systems, Speed governing system, Hydraulic valve actuator, Turbine generator response, Static performance of speed governor, Closing of ALFC loop, Concept of control area, Static response of primary ALFC loop, Integral control, ALFC of multi-control area systems (POOL operation).The Two-Area system, Modeling the Tie-Line, Block Diagram representation of Two-Area system, Static response of Two-Area system and Tie-Line Bias control.

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL 16/9/2010
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

12.Hours

UNIT - 4
CONTROL OF VOLTAGE AND REACTIVE POWER: Introduction, generation and absorption of reactive power, relation between voltage, power and reactive power at a node, single machine infinite bus systems, methods of voltage control, sub synchronous resonance, voltage stability, voltage collapse.
6 Hours

PART - B

UNIT - 5
OPTIMAL SYSTEM OPERATION AND UNIT COMMITMENT: Introduction , Optimal operation of generators on a bus bar, Statement of the Unit Commitment problem, need and importance of unit commitment, Constraint in Unit Commitment, Unit Commitment solution methods-Priority lists method, Forward Dynamic Programming method(excluding problem), Spinning reserve. 6 Hours

UNIT - 6
POWER SYSTEM SECURITY: Introduction, factors affecting power system security, Security analysis, Contingency Selection, Techniques for contingency evaluation-D.C. load flow and fast decoupled load flow.
6 Hours

UNIT 7
SYSTEM MONITORING AND CONTROL: Introduction , Energy management system, the basis of power system state estimation(PSSE), mathematical description of PSSE process, minimization technique for PSSE, Least Square estimation, Error and detection in PSSE, System security and emergency control.
6 Hours

UNIT- 8
POWER SYSTEM RELIABILITY: Introduction, Modes of failures of a system, Generating system and its performance, derivation of reliability index, reliability measure for N- unit system, cumulative probability outages- Recursive Relation, Loss of load probability, Frequency and duration of a state.
8 Hours

Text Books:

1. Modern Power System Analysis- I J Nagarath and D P Kothari, TMH, 3rd Edition, 2003
2. Electrical Energy Systems Theory, O.I Elgerd, TMH,2008.
3. Power generation, operation and control- Allen J Wood & Woollenberg, John Wiley and Sons, Second Edition, 2009.
4. Electric Power Systems- B.M.Weedy and B.J. Cory, Wiley student edition, 1999
5. Computer Aided Power System Operation and Analysis- R.N. Dhar, Tata McGraw-Hill, 1987.

REFERENCE:

1. Computer Aided Power System Analysis- G.L.Kusic, PHI,2010.
2. Power System Analysis, Operation and Control, Abhijit Chakrabarti and Sunita Halder, PHI, Second Edition, 2009
3. Power system stability and control, Prabha Kundur, TMH, 9th reprint, 2007.

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL 18/9/2015
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

UNIT - 7

ENERGY FROM OCEAN: Tidal Energy – Principle of Tidal Power, Components of Tidal Power Plant (TPP), Classification of Tidal Power Plants, Estimation of Energy – Single basin and Double basin type TPP (no derivations, Simple numerical problems), Advantages and Limitations of TPP. Ocean Thermal Energy Conversion (OTEC): Principle of OTEC system, Methods of OTEC power generation – Open Cycle (Claude cycle), Closed Cycle (Anderson cycle) and Hybrid cycle (block diagram description of OTEC); Site-selection criteria, Biofouling, Advantages & Limitations of OTEC. 6 Hours

UNIT - 8

EMERGING TECHNOLOGIES: Fuel Cell, Small Hydro Resources, Hydrogen Energy, and Wave Energy. (Principle of Energy generation using block diagrams, advantages and limitations). 6 Hours

TEXT BOOKS:

1. Non-Conventional Sources of Energy,Rai, G. D, Khanna Publishers, 4th Edition, 2007
2. Non-Conventional Energy Resources, Khan, B. H., TMH, 2nd Edition.

REFERENCE BOOK:

1. Fundamentals of Renewable Energy Systems, Mukherjee, D and Chakrabarti, S., New Age International Publishers, 2005.

10EE63 ELECTRICAL MACHINE DESIGN

Subject Code	:	10EE63	IA Marks	:	25
No. of Lecture Hrs / Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART - A

UNIT - 1

PRINCIPLES OF ELECTRICAL MACHINE DESIGN: Introduction, considerations for the design of electrical machines, limitations. Different types of materials and insulators used in electrical machines. 4 Hours

UNIT - 2

DESIGN OF DC MACHINES: Output equation, choice of specific loadings and choice of number of poles, design of Main dimensions of the DC machines, Design of armature, Opt dimensions, commutator and brushes, magnetic circuit - estimation of ampere turns, design of yoke and poles- main and inter poles, field windings – shunt, series and inter poles. 10 Hours

UNIT - 3 & 4

DESIGN OF TRANSFORMERS (Single phase and three phase): Output equation for single phase and three phase transformers, choice of specific loadings, expression for volts/turn, determination of main dimensions of the core, types of windings and estimation of number of turns and conductor cross sectional area of Primary and secondary windings, estimation of no load current, expression for leakage reactance and voltage regulation. Design of tank and cooling tubes (round and rectangular) 12 Hours

PART - B

UNIT - 5 & 6

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

DESIGN OF INDUCTION MOTORS: Output equation, Choice of specific loadings, main dimensions of three phase induction motor, Stator winding design, choice of length of the air gap, estimation of number of slots for the squirrel cage rotor, design of Rotor bars and end ring, design of Slip ring induction motor, estimation of No load current and leakage reactance, and circle diagram. 14 Hours

UNIT - 7 & 8

DESIGN OF SYNCHRONOUS MACHINES: Output equation, Choice of specific loadings, short circuit ratio, design of main dimensions, armature slots and windings, slot details for the stator of salient and non salient pole synchronous machines. Design of rotor of salient pole synchronous machines, magnetic circuits, dimensions of the pole body, design of the field winding, and design of rotor of non-salient pole machine. 12 Hours

TEXT BOOKS:

1. A Course In Electrical Machine Design, A.K.Sawhney,Dhanpatt Rai & Sons
2. Design Of Electrical Machines, V. N. Mittle, 4th edition

REFERENCE BOOKS:

1. Performance And Design Of AC Machines, M.G.Say,CBS Publishers and Distributors Pvt.Ltd.
2. Design Data Handbook, A.Shanmugasundaram, G,Gangadharan,R.Palani,Wiley Eastern Ltd.

10EE46 TRANSFORMERS AND INDUCTION MACHINES

Subject Code.	:	10EE46	IA Marks	:	25
No. of Lecture Hrs./ Week	:	04	Exam Hours	:	03
Total No. of Lecture Hrs.	:	52	Exam Marks	:	100

PART – A

UNIT 1:

Basic Concepts: Principle of operation of transformer, Constructional details of shell type and core type single-phase and three-phase transformers. EMF equation, operation of practical power transformer under

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY
NAVODAYA NAGAR, BIJENGERA ROAD, RAICHUR-584103
(Affiliated to Visvesvaraya Technological University, Belgaum)

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

CERTIFICATE

Certified that the project work entitled "UNDERGROUND CABLE FAULT DISTANCE LOCATOR" carried out by NIVEDITHA (3NA13EE402), RAMACHANDRA REDDY M (3NA13EE403), SANTOSH KUMAR G (3NA13EE405), SHRUTI K (3NA13EE408) are bonafide students of NAVODAYA INSTITUTE OF TECHNOLOGY, RAICHUR in partial fulfillment for the award of **Bachelor of Engineering** in **Electrical and Electronics Engineering** of the Visvesvaraya Technological University, Belgaum during the year **2015-2016**. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Guide	HOD	Principal
(Prof. Daniel.N)	(Dr. Srinivasan.M.)	(Dr. ShivaPrakash.C.K)

External Viva

Name of the Examiners:	Signature with Date
1.	
2.	

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103, Karnataka

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ABSTRACT

This project proposes fault location model for underground power cable using microcontroller. The aim of this project is to determine the distance of underground cable fault from base station in kilometers. This project uses the simple concept of ohm's law. When any fault like short circuit occurs, voltage drop will vary depending on the length of fault in cable, since the current varies. A set of resistors are therefore used to represent the cable and a dc voltage is fed at one end and the fault is detected by detecting the change in voltage using an analog to digital converter and a microcontroller is used to make the necessary calculations so that the fault distance is displayed on the LCD display.

Head of the Department
Department of Electrical and
Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103. Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY
RAICHUR

PRINCIPAL 18/9/2020
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER 1

INTRODUCTION

Power supply networks are growing continuously and their reliability is getting more important than ever. The complexity of the whole network comprises numerous components that can fail and interrupt the power supply for the end user. For most of the worldwide operated low voltage and medium voltage distribution lines underground cables have been used for many decades. During the last years, also high voltage lines have been developed to cables. To reduce the sensitivity of distribution networks to environmental influences underground high voltage cables are used more and more. They are not influenced by weather conditions, heavy rain, storm, snow and ice as well as pollution. Even the technology used in cable factories is improving steadily certain influences may cause cables to fail during operation or test. Cables have been in use for over 80years. The number of different designs as well as the variety of cable types and accessories used in a cable network is large. The ability to determine all kind of different faults with widely different fault characteristics is turning on the suitable measuring equipment as well as on the operator's skills. The right combination enables to reduce the expensive time that is running during a cable outage to a minimum.

Till last decades cables were made to lay overhead& currently it is lay to underground cable which is superior to earlier method. Because the underground cable are not affected by any adverse weather condition such as storm, snow, heavy rainfall as well as pollution. But when any fault occur in cable, then it is difficult to locate fault. So we will move to find the exact location of fault.

Now the world is become digitalized so the project is intended to detect the location of fault in digital way. The underground cable system is more common practice followed in many urban areas. While fault occurs for some reason, at that time the repairing process related to that particular cable is difficult due to not knowing the exact location of cable fault.

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103. Karnataka

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER 2

BLOCK DIAGRAM

Below shown figure is the block diagram of underground cable fault distance locator.

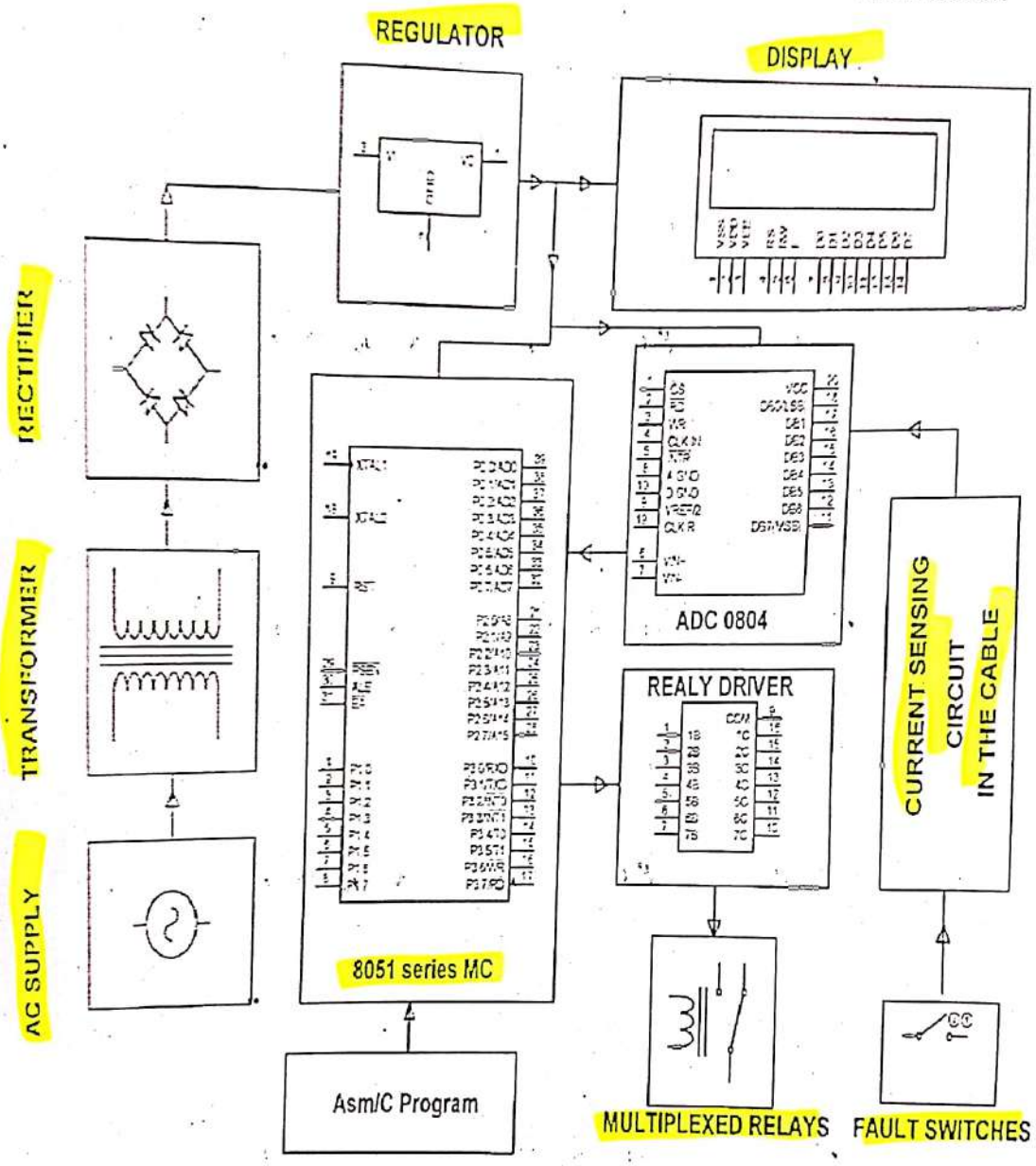


Fig 3(a): block diagram

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103. Karnataka

PRINCIPAL
Navodaya Institute of Technology (NIT,
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Scanned with CamScanner

CHAPTER 3

HARDWARE REQUIREMENTS

HARDWARE COMPONENTS:

1. TRANSFORMER (230 – 6/0/6 V AC)
2. VOLTAGE REGULATOR (LM 7805& LM 7812)
3. RECTIFIER
4. FILTER
5. MICROCONTROLLER (AT89S52)
6. LIQUID CRYSTAL DISPLAY
7. ADC0804
8. ULN2003
9. RELAYS
10. IN4007
11. RESISTOR
12. CAPACITOR

Head of the Department
Department of Electrical and Electronics Engineering
Navodaya Institute of Technology,
RAICHUR-584 103. Karnataka

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

PRINCIPAL 16/9/14
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

CHAPTER 4

4.1FAULT LOCATION METHODS

Fault location methods can be classified as:

1) Online method: These methods utilize& process the sampled voltages& current to determine the fault points. Online methods for underground cable are less than overhead lines.

2) Offline method: In this method special instrument is used to test out service of cable in the field. There are two offline methods as following

- **Tracer method:** In this method fault point is detected by walking on the cable lines. Fault point is indicated from audible signal or electromagnetic signal. It is used to pinpoint fault location very accurately.
- **Terminal method:** It is a technique used to detect fault location of cable from one or both ends without tracing. This method use to locate general area of fault. to expedite tracing on buried cable.
- **Pre-location:** Pre-location is used to determine the fault distance. There are predominantly two methods for this.

  - **Pulse reflection method:** A pulse induced at the starting end of the cable reaches the cable fault with a speed of v/2 and is there reflected back toward the starting end of the cable. The elapsed time multiplied by the diffusion speed v/2 gives the distance to the source of the fault. See also: Time-domain reflectometer.
  - **Transient method:** In the transient method, a breakdown is triggered at the cable fault. This effects a low-resistance short circuit for a few milliseconds. This in turn produces two travelling waves diffusing in opposite directions. These waves are reflected at the cable ends so that they then travel toward each other again in the direction of the cable fault. The waves are unable to pass the fault because of the arc produced by the short circuit, so they are therefore reflected back again as in the pulse reflection method, which due to the burning short circuit, results in reversal of polarity.

Mechanical Engineering

of business opportunities: Market Feasibility Study; Technical Feasibility Study; Financial Feasibility Study & Social Feasibility Study.

7 Hours

TEXT BOOKS:

1 **Principles of Management** – P. C.Tripathi, P.N. Reddy – Tata McGraw Hill,
2 **Dynamics of Entrepreneurial Development & Management** Vasant Desai - Himalaya Publishing House
3 **Entrepreneurship Development** – Poornima. M. Charantimath Small Business Enterprises - Pearson Education - 2006 (2 & 4).

REFERENCE BOOKS:

1 **Management Fundamentals** - Concepts, Application, Skill Development - Robers Lusier - Thomson
2 **Entrepreneurship Development** - S.S.Khanka - S.Chand & Co.
3 **Management** - Stephen Robbins - Pearson Education/PHI - 17th Edition, 2003.

DESIGN OF MACHINE ELEMENTS-I

Subject Code	**: 10ME52**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART – A

UNIT- 1

Introduction: Definitions: normal, shear, biaxial and tri axial stresses, Stress tensor, Principal Stresses. Engineering Materials and their mechanical properties, Stress-Strain diagrams, Stress Analysis, Design considerations: Codes and Standards.

05 Hours

UNIT- 2

Design For Static & Impact Strength:

Static Strength: Static loads and factor of safety, Theories of failure: Maximum normal stress theory, Maximum shear stress theory, Maximum strain theory, Strain energy theory, Distortion energy theory. Failure of brittle and ductile materials, Stress concentration, Determination of Stress concentration factor.

Impact Strength: Introduction, Impact stresses due to axial, bending and torsional loads, effect of inertia.

07 Hours

UNIT - 3

Design For Fatigue Strength: Introduction- S-N Diagram, Low cycle fatigue, High cycle fatigue, Endurance limit, Modifying factors: size effect, surface effect, Stress concentration effects, Fluctuating stresses, Goodman and Soderberg relationship, stresses due to combined loading, cumulative fatigue damage.

08 Hours

UNIT - 4

Threaded Fasteners: Stresses in threaded fasteners, Effect of initial tension, Design of threaded fasteners under static, dynamic and impact loads, Design of eccentrically loaded bolted joints.

06 Hours

PART – B

UNIT - 5

Design Of Shafts: Torsion of shafts, design for strength and rigidity with steady loading, ASME codes for power transmission shafting, shafts under fluctuating loads and combined loads.

07 Hours

UNIT - 6

Cotter And Knuckle Joints, Keys And Couplings: Design of Cotter and Knuckle joints, Keys: Types of keys, Design of keys, Couplings: Rigid and flexible couplings, Flange coupling, Bush and Pin type coupling and Oldham's coupling.

07 Hours

UNIT - 7

Riveted and Welded Joints – Types, rivet materials, failures of riveted joints, Joint Efficiency, Boiler Joints, Lozanze Joints, Riveted Brackets. Welded Joints – Types, Strength of butt and fillet welds, eccentrically loaded welded joints.

07 Hours

UNIT - 8

Power Screws: Mechanics of power screw, Stresses in power screws, efficiency and self-locking, Design of Power Screw, Design of Screw Jack: (Complete Design).

05 Hours

TEXT BOOKS:

1. **Mechanical Engineering Design,** Joseph E Shigley and Charles R. Mischke. McGraw Hill International edition, 6th Edition 2009.
2. **Design of Machine Elements,** V.B. Bhandari, Tata McGraw Hill Publishing Company Ltd., New Delhi, 2nd Edition 2007.

DESIGN DATA HANDBOOK:

1. **Design Data Hand Book,** K. Lingaiah, McGraw Hill, 2nd Ed.
2. **Data Hand Book,** K. Mahadevan and Balaveera Reddy, CBS Publication
3. **Design Data Hand Book,** H.G. Patil, I. K. International Publisher, 2010.

REFERENCE BOOKS:

1. **Machine Design,** Robert L. Norton, Pearson Education Asia, 2001.
2. **Design of Machine Elements,** M. F. Spotts, T. E. Shoup, L. E. Hornberger, S. R. Jayram and C. V. Venkatesh, Pearson Education, 2006.
3. **Machine Design,** Hall, Holowenko, Laughlin (Schaum's Outlines series) Adapted by S.K. Somani, Tata McGraw Hill Publishing Company Ltd., New Delhi, Special Indian Edition, 2008.
4. **Fundamentals of Machine Component Design,** Robert C. Juvinall and Kurt M Marshek, Wiley India Pvt. Ltd., New Delhi, 3rd Edition, 2007.

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology
RAICHUR-584 103

Lambert's law; radiation heat exchange between two finite surfaces-configuration factor or view factor. Numerical problems.

07 Hours

TEXT BOOKS:

1. **Heat & Mass transfer,** Tirumaleshwar, Pearson education 2006
2. **Heat transfer-A basic approach,** Ozisik, Tata McGraw Hill 2002

REFERENCE BOOKS:

1. **Heat transfer, a practical approach,** Yunus A- Cengel Tata Mc Graw Hill
2. **Principles of heat transfer,** Kreith Thomas Learning 2001
3. **Fundamentals of heat and mass transfer,** Frenk P. Incropera and David P. Dewitt, John Wiley and son's.
4. **Heat transfer,** P.K. Nag, Tata McGraw Hill 2002.

FINITE ELEMENT METHODS

Subject Code	**: 10ME64**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART-A

UNIT-1

Introduction: Equilibrium equations in elasticity subjected to body force, traction forces, and stress-strain relations for plane stress and plane strains. General description of Finite Element Method, Application and limitations. Types of elements based on geometry. Node numbering, Half band width.

07 Hours

UNIT-2

Basic Procedure: Euler - Lagrange equation for bar, beam (cantilever / simply supported fixed) Principle of virtual work, principle of minimum potential energy, Raleigh's Ritz method. Direct approach for stiffness matrix formulation of bar element. Galerkin's method.

07 Hours

UNIT-3

Interpolation Models: Interpolation polynomials- Linear, quadratic and cubic. Simplex complex and multiplex elements. 2D PASCAL's triangle. CST elements-Shape functions and Nodal load vector, Strain displacement matrix and Jacobian for triangular and rectangular element.

07 Hours

UNIT-4

Solution of 1-D Bars: Solutions of bars and stepped bars for displacements, reactions and stresses by using penalty approach and elimination approach. Guass-elimination technique.

06 Hours

PART-B

UNIT-5

Higher Order Elements: Langrange's interpolation, Higher order one dimensional elements-Quadratic and cubic element and their shape functions. Shape function of 2-D quadrilateral element-linear, quadric element Iso-parametric, Sub parametric and Super parametric elements. numerical integration : 1, 2 and 3 gauge point for 1D and 2D cases.

06 Hours

UNIT-6

Trusses: Stiffness matrix of Truss element. Numerical problems.

06 Hours

UNIT-7

Beams: Hermite shape functions for beam element, Derivation of stiffness matrix. Numerical problems of beams carrying concentrated, UDL and linearly varying loads.

06 Hours

UNIT-8

Heat Transfer: Steady state heat transfer, 1D heat conduction governing equations. Functional approach for heat conduction. Galerkin's approach for heat conduction. 1D heat transfer in thin fins.

07 Hours

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

TEXT BOOKS:

1. **Finite Elements in Engineering**, T.R.Chandrupatla, A.D Belegunde, 3rd Ed PHI.
2. **Finite Element Method in Engineering**, S.S. Rao, 4th Edition, Elsevier, 2006.

REFERENCE BOOKS:

1. **"Finite Element Methods for Engineers"** U.S. Dixit, Cengage Learning, 2009
2. **Concepts and applications of Finite Element Analysis**, R.D. Cook D.S Maltus, M.E Plesha, R.J.Witt, Wiley 4th Ed, 2009
3. **Finite Element Methods**, Daryl. L. Logon, Thomson Learning 3rd edition, 2001.
4. **Finite Element Method**, J.N.Reddy, McGraw -Hill International Edition.

MECHATRONICS & MICROPROCESSOR

Subject Code	**: 10ME65**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART - A

UNIT - 1

Introduction to Mechatronic Systems: Measurement and control systems Their elements and functions, Microprocessor based controllers.

06 Hours

UNIT - 2

Review of Transducers and Sensors: Definition and classification of transducers. Definition and classification of sensors. Principle of working and applications of light sensors, proximity sensors and Hall effect sensors.

07 Hours

TEXT BOOKS:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers.
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

REFERENCE BOOKS:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers.

MATERIAL SCIENCE AND METALLURGY

Subject Code	**: 10ME32A /42A**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART – A

UNIT - 1

Crystal Structure: BCC, FCC and HCP Structures, coordination number and atomic packing factors, crystal imperfections -point line and surface imperfections. Atomic Diffusion: Phenomenon, Ficks laws of diffusion, factors affecting diffusion.

06 Hours

UNIT - 2

Mechanical Behaviour: Stress-strain diagram showing ductile and brittle behaviour of materials, linear and non linear elastic behaviour and properties, mechanical properties in plastic range, yield strength offset yield strength, ductility, ultimate tensile strength, toughness. Plastic deformation of single crystal by slip and twinning.

06 Hours

UNIT - 3

Fracture: Type I, Type II and Type III.

Creep: Description of the phenomenon with examples. three stages of creep, creep properties, stress relaxation.

Fatigue: Types of fatigue loading with examples, Mechanism of fatigue, fatigue properties, fatigue testing and S-N diagram.

07 Hours

UNIT - 4

Solidification: Mechanism of solidification, Homogenous and Heterogeneous nucleation, crystal growth, cast metal structures.

Phase Diagram I: Solid solutions Hume Rothary rule substitutional, and interstitial solid solutions, intermediate phases, Gibbs phase rule.

07 Hours

PART - B

UNIT - 5

Phase Diagram II: Construction of equilibrium diagrams involving complete and partial solubility, lever rule. Iron carbon equilibrium diagram description of phases, solidification of steels and cast irons, invariant reactions.

06 Hours

UNIT - 6

Heat treating of metals: TTT curves, continuous cooling curves, annealing and its types. normalizing, hardening, tempering, martempering, austempering, hardenability, surface hardening methods like carburizing, cyaniding, nitriding, flame hardening and induction hardening, age hardening of aluminium-copper alloys.

07 Hours

UNIT - 7

Ferrous and non ferrous materials: Properties, Composition and uses of

- Grey cast iron, malleable iron, SG iron and steel
- Copper alloys-brasses and bronzes.
  Aluminium alloys-Al-Cu,Al-Si,Al-Zn alloys.

06 Hours

INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

MECHANICS OF COMPOSITE MATERIALS

Subject Code	: 10ME662	IA Marks	: 25
Hours/Week	: 04	Exam Hours	: 03
Total Hours	: 52	Exam Marks	: 100

PART – A

UNIT - 1

Introduction To Composite Materials: Definition, classification and characteristics of composite Materials – fibrous composites, laminated composites, particulate composites.

Applications: Automobile, Aircrafts, missiles. Space hardware, Electrical and electronics, Marine, recreational and sports equipment, future potential of composites.

06 Hours

UNIT - 2

Fiber Reinforced Plastic Processing: Lay up and curing, fabricating process, open and closed mould process, hand lay up techniques; structural laminate bag molding, production procedures for bag molding; filament winding, pultrusion, pulforming, thermo-forming, injection molding, blow molding.

07 Hours

UNIT - 3

Micro Mechanical Analysis of a Lamina: Introduction, Evaluation of the four elastic moduli by Rule of mixture, Numerical problems. **Macro Mechanics of a Lamina:** Hooke's law for different types of materials, Number of elastic constants, Two - dimensional relationship of compliance and stiffness matrix.

07 Hours

UNIT – 4.

Macro Mechanics of a Lamina Hooke's law for two-dimensional angle lamina, engineering constants - Numerical problems. Stress-Strain relations for lamina of arbitrary orientation, Numerical problems.

06 Hours

PART – B

UNIT – 5

Biaxial Strength Theories: Maximum stress theory, Maximum strain theory, Tsai-Hill theory, Tsai, Wu tensor theory, Numerical problems.

06 Hours

UNIT – 6

Macro Mechanical Analysis of Laminate: Introduction, code, Kirchoff hypothesis, CL T, A, B, and D matrices (Detailed derivation) , Special cases of laminates, Numerical problems.

06 Hours

UNIT - 7

Metal Matrix Composites: Reinforcement materials, types, characteristics and selection base metals selection. Need for production MMC's and its application.

Fabrication Process For MMC's: Powder metallurgy technique, liquid metallurgy technique and secondary processing, special fabrication techniques.

07 Hours

UNIT - 8

STUDY PROPERTIES OF MMC'S: Physical Mechanical, Wear, machinability and Other Properties. Effect of size, shape and distribution of particulate on properties.

07 Hours

TEXT BOOKS:

1. **Composite Science and Engineering,** K. K. Chawla Springer Verlag 1998.
2. **Mechanics of composite materials,** Autar K. Kaw CRC Press New York.

REFERENCE BOOKS:

1. **Fiber Reinforced Composites,** P. K. Mallick, Marcel Dekker,Inc
2. **Mechanics of Composite Materials,** Robert M. Jones, McGraw Hill Kogakusha Ltd.1998

METALLOGRAPHY AND MATERIAL TESTING LABORATORY

Subject Code	**: 10MEL37A / 47A**	**IA Marks**	**: 25**
Hours/Week	**: 03**	**Exam Hours**	**: 03**
Total Hours	**: 48**	**Exam Marks**	**: 50**

PART – A

1. Preparation of specimen for Metallograpic examination of different engineering materials. Identification of microstructures of plain carbon steel, tool steel, gray C.I, SG iron, Brass, Bronze & composites.
2. Heat treatment: Annealing, normalizing, hardening and tempering of steel. Hardness studies of heat-treated samples.
3. To study the wear characteristics of ferrous, non-ferrous and composite materials for different parameters.
4. Non-destructive test experiments like,
   (a). Ultrasonic flaw detection
   (b). Magnetic crack detection
   (c). Dye penetration testing. To study the defects of Cast and Welded specimens

PART – B

1. Tensile, shear and compression tests of metallic and non metallic specimens using Universal Testing Machine
2. Torsion Test
3. Bending Test on metallic and nonmetallic specimens.
4. Izod and Charpy Tests on M.S, C.I Specimen.
5. Brinell, Rockwell and Vickers's Hardness test.
6. Fatigue Test.

Scheme of Examination:

ONE question from part -A:	**20** Marks
ONE question from part -B:	**20** Marks
Viva -Voice:	**10** Marks
Total :	**50** Marks

ELECTIVE-I (GROUP - A)

THEORY OF ELASTICITY

Subject Code	**: 10ME661**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART – A

UNIT - 1

Definition And Notation: Stress, Stress at a Point, Equilibrium Equations, Principal Stresses, Mohr's Diagram, Maximum Shear Stress, Boundary Conditions.

6 Hours

UNIT - 2

Strain At A Point: Compatibility Equations, Principal Strains, Generalised Hooke's law, Methods of Solution of Elasticity Problems – Plane Stress-Plane Strain Problems.

7 Hours

UNIT - 3

Two Dimensional Problems: Cartesian co-ordinates – Airy's stress functions – Investigation of Airy's Stress function for simple beam problems – Bending of a narrow cantilever beam of rectangular cross section under edge load – method of Fourier analysis – pin ended beam under uniform pressure.

7 Hours

UNIT - 4

General Equations In Cylindrical Co-Ordinates: Thick cylinder under uniform internal and / or external pressure, shrink and force fit, stress concentration.

6 Hours

PART – B

UNIT - 5

Stresses In An Infinite Plate (with a circular hole) subjected to uniaxial and biaxial loads, stress concentration, stresses in rotating discs and cylinders.

7 Hours

UNIT - 6

Torsion Of Circular, Elliptical And Triangular Bars: membrane analogy, torsion of thin open sections and thin tubes.

6 Hours

UNIT - 7

Thermal Stresses: Thermo elastic stress strain relationship, Equations of equilibrium Thermal stresses in thin circular discs and in long circular cylinder, sphere.

7 Hours

UNIT - 8

Uniqueness Theorem: Principle of super position, reciprocal theorem, saint venant principle.

6 Hours

TEXT BOOKS:

1. **Advanced Mechanics of solids**, L. S. Srinath, Tata Mc. Graw Hill, 2003
2. **Theory of Elasticity**, S. P. Timoshenko and J. N Gordier, Mc.Graw Hill International, 3rd edition, 1972

REFERENCES BOOKS:

1. **Theory of Elasticity**, Dr. Sadhu Singh, Khanna Publications, 1988
2. **Elasticity, Theory, Applications & Numericals**, Martin H Sadd, Elsevier. 2005
3. **Applied Elasticity**, Seetharamu & Govindaraju, Interline Publishing
4. **Applied Elasticity**, C.T. WANG Sc. D. McGraw Hill Book Co.1953

REFERENCE BOOKS:

1. **Thermodynamics**, An Engineering Approach, Yunus A.Cenegal and Michael A.Boles, Tata McGraw Hill publications, 2002
2. **Engineering Thermodynamics**, J.B.Jones and G.A.Hawkins, John Wiley and Sons..
3. **Fundamentals of Classical Thermodynamics**, G.J.Van Wylen and R.E.Sonntag, Wiley Eastern.
4. **An Introduction to Thermodynamcis**, Y.V.C.Rao, Wiley Eastern, 1993,
5. **B.K Venkanna, Swati B. Wadavadagi "Basic Thermodynamics,** PHI, New Delhi, 2010

MECHANICS OF MATERIALS

Subject Code	**: 10ME34**	**IA Marks**	**: 25**
Hours/Week	**: 04**	**Exam Hours**	**: 03**
Total Hours	**: 52**	**Exam Marks**	**: 100**

PART-A

UNIT 1:

Simple Stress and Strain: Introduction, Stress, strain, mechanical properties of materials, Linear elasticity, Hooke's Law and Poisson's ratio, Stress-Strain relation - behaviour in tension for Mild steel, cast iron and non ferrous metals. Extension / Shortening of a bar, bars with cross sections varying in steps, bars with continuously varying cross sections (circular and rectangular), Elongation due to self weight, Principle of super position.

07 Hours

UNIT 2:

Stress in Composite Section: Volumetric strain, expression for volumetric strain, elastic constants, simple shear stress, shear strain, temperature stresses (including compound bars).

06 Hours

UNIT 3:

Compound Stresses: Introduction, Plane stress, stresses on inclined sections, principal stresses and maximum shear stresses, Mohr's circle for plane stress.

07 Hours

UNIT 4:

Energy Methods: Work and strain energy, Strain energy in bar/beams, Castiglinios theorem, Energy methods.

Thick and Thin Cylinder Stresses in thin cylinders, changes in dimensions of cylinder (diameter, length and volume). Thick cylinders Lame's equation (compound cylinders not included).

06 Hours

PART-B

UNIT 5:

Bending Moment and Shear Force in Beams: Introduction, Types of beams, loads and reactions, shear forces and bending moments, rate of loading, sign conventions, relationship between shear force and bending moments. Shear force and bending moment diagrams for different beams subjected to concentrated loads, uniformly distributed load, (UDL) uniformly varying load (UVL) and couple for different types of beams.

07 Hours

UNIT 6:

Bending and Shear Stresses in Beams: Introduction, Theory of simple bending, assumptions in simple bending. Bending stress equation, relationship between bending stress, radius of curvature, relationship between bending moment and radius of curvature. Moment carrying capacity of a section. Shearing stresses in beams, shear stress across rectangular, circular, symmetrical I and T sections. (composite / notched beams not included).

07 Hours

UNIT 7:

Deflection of Beams: Introduction, Differential equation for deflection. Equations for deflection, slope and bending moment. Double integration

INSTITUTE OF TECHNOLOGY RAICHUR

Head of Department
Mechanical Engineering
Navodaya Institute of Technology
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY
BIJJANAGERA ROAD, RAICHUR-584103
(Affiliation VTU Belgaum)

DEPARTMENT OF MECHANICAL ENGINEERING

CERTIFICATE

Certified that the project work entitled **"FATIGUE LIFE ESTIMATION OF AIRCRAFT WING STRUCTURE USING ANSYS"** carried out by **RIZWANA BEGUM (3NA13ME413), SHANKAR DURGAD (3NA13ME415), SHANTAPPA.S.MASALI (3NA13ME416), SHARANAKUMAR NUCHHI (3NA13ME417)** a bonafide student of Navodaya Institute of Technology, Raichur in partial fulfillment for the award of Bachelor of Engineering in Mechanical Engineering of the Visvesvaraiya Technological University, Belgaum, during the year 2015-2016. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Signature of the Guide	Signature of the HOD	Signature of the Principal
Asst Prof. **SRIKAR.G.KULKARNI**	**Dr.P.RATHNA KUMAR** **Head of Department** **Department of Mechanical Engineering** **Navodaya Institute of Technology (NIT)** **RAICHUR.**	**Dr. C.K SHIVA PRAKASH**

External Viva

Name of the examiners	Signature with date
1. Dr. P. RATHNA KUMAR	
2.	

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

ABSTRACT

Fatigue is progressive failure mechanism and material degradation initiates with the first cycle. The degradation/damage accumulation progresses until a finite crack is nucleated, then the crack propagates until the failure process culminates in a complete failure of the structures. The total life from first cycle to the complete failure can be divided into three stages: Initial life interval, Life interval, Final Life interval. The fatigue damage is mainly based on two designs: FAIL-SAFE and SAFE-LIFE. The objective is to design a Fail-Safe Structural component. In this project we have designed a Wing-Bracket interaction which was not yet designed by any of the industry. And we have estimated the fatigue life of our Wing-Bracket attachment model. Here we compared the fatigue life of our model with three materials such as Managing Steel, Titanium and Structural A36 steel. Among this three we have proved that Managing steel gives more fatigue life compared to other two materials. For estimating the fatigue life we have made some hand calculations.

Finally we have represented the fatigue life with the help of Goodman Curve. The Structural Component is designed and analysed using CATIA and ANSYS Softwares. In analysis the maximum stress at which the component undergoes degradation/damage is calculated for different End Conditions (loadings and stresses), which determines the fatigue life of the component.

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY * RAICHUR

CONTENT

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR

2 Create 2d sketch on XY-Plane, because airfoil coordinate I've created in spreadsheet was based on XY plane. Then import point into it (NACA4412). As shown in fig

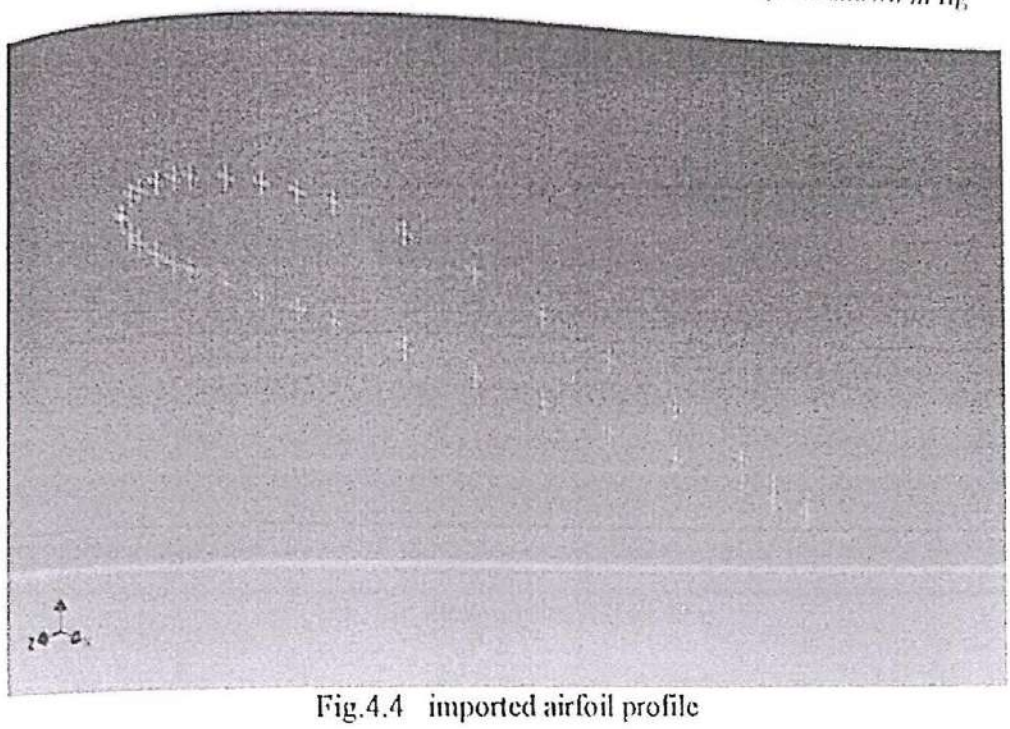


Fig.4.4 imported airfoil profile

3. Use spline to connect every point together to form close loop sketch. And then closesketch.

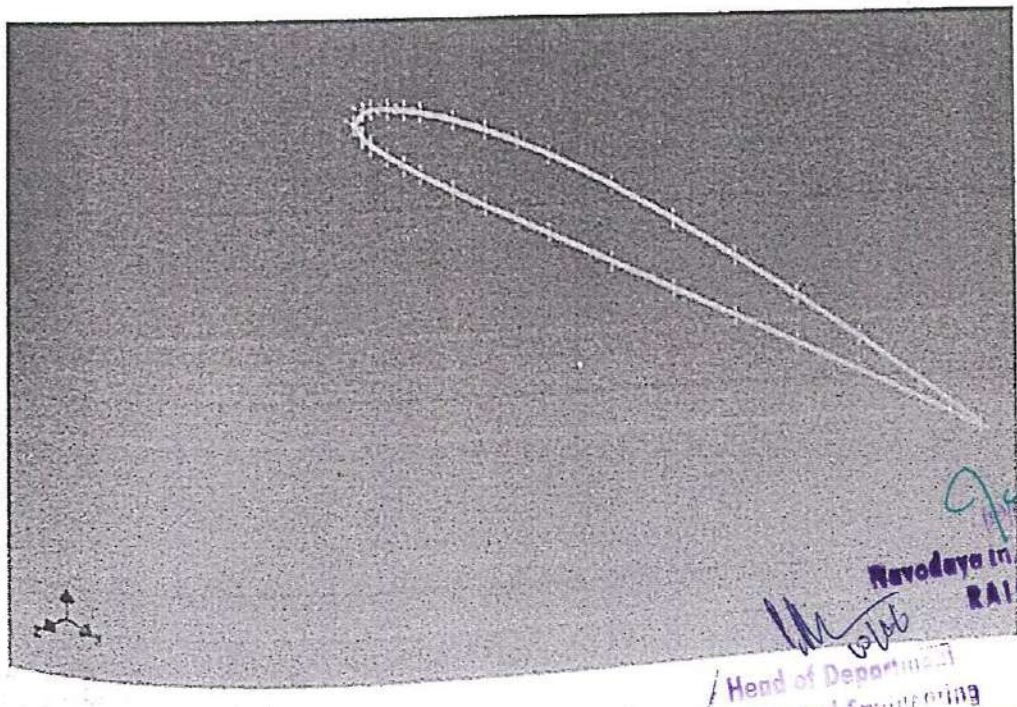


Fig.4.5 Generated airfoil wing

5.3 Fatigue regimes

Based on the number of stresses or strain cycles that the part is expected to undergo in its life, it is divided either a Low cycle regime (LCF) or a High cycle regime (HCF). There is no sharp dividing line between these two regimes. Many of them suggests that $N=10^3$ cycles is the reasonable approximation of divide between HCF and LCF.

High cycle fatigue(HCF) is the region beyond $N=10^3$ cycles. It is based on the assumptions that the part behaves elastically ignoring occurrence of plastic deformation. Disadvantage of high cycle fatigue is that the slope of the S-N curve is so small that accurate results are difficult to obtain. This module calculates the fatigue life of the part under constant amplitude fluctuating loading assuming stress range controls fatigue life. Fatigue strength of the material is known in high cycle fatigue by three empirical relationships:

- Goodman relationship.
- Gerber relationship.
- Soderberg relationship.

Low cycle fatigue (LCF) is the region below $N=10^3$ cycles. It is necessary to investigate the behavior of the material subjected to cyclic deformation. This model calculate the fatigue life of a part under constant amplitude fluctuating loading assuming strain range controls fatigue life.

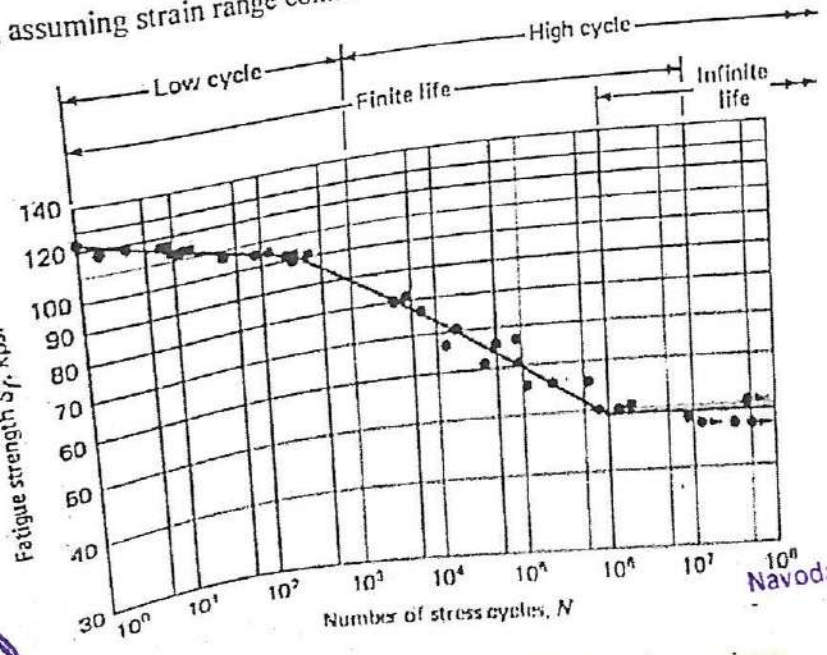


Fig.5.3 S-N diagram for showing various fatigue regimes

6.RESULTS AND REVIEWS

The results are viewed In ANSYS general postprocessor phase. Here the behavior of the model in different loading conditions can be examined very accurately. Here we are viewing the difference between the deformed and un-deformed shapes as shown in fig(6.1). Here we are mainly dealing with the von Mises stress, which take the account of the mean stress in the model.

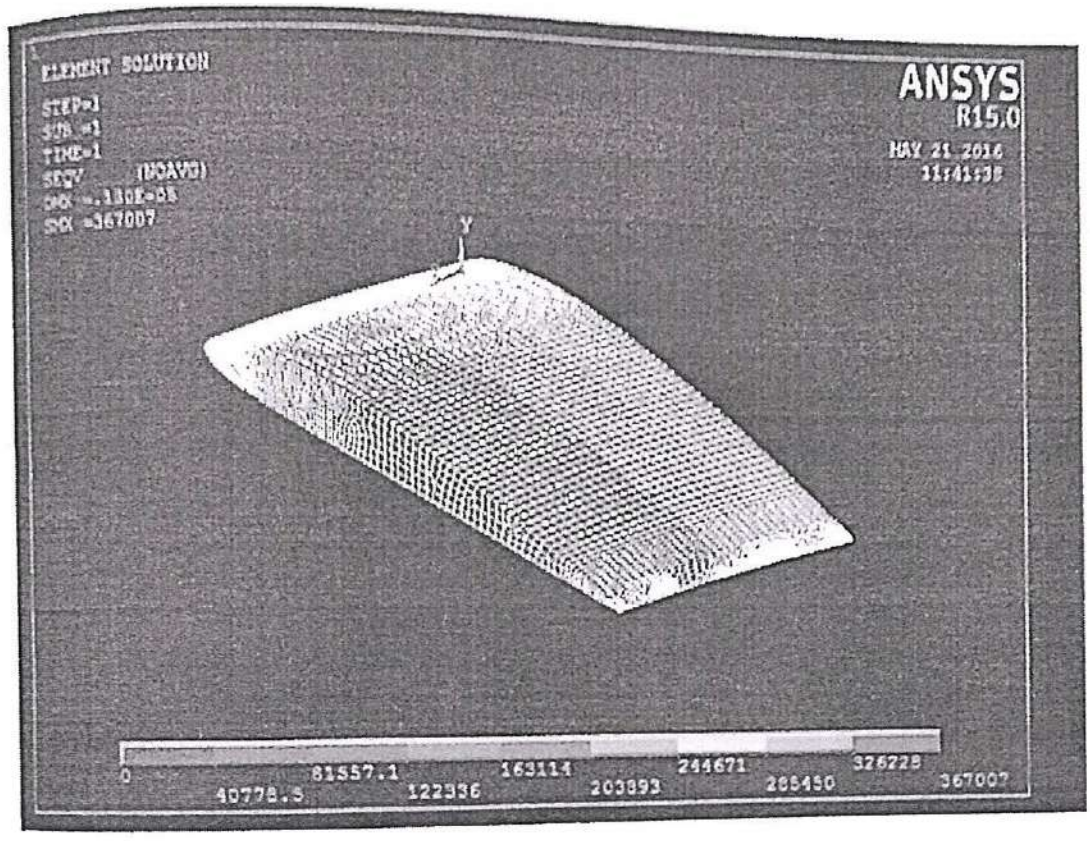


Fig. 6.1 Element solution of aircraft wing

6.1 Von Mises stress

The von misescriterian is an experimentally based law that can be used to determine the whether the stress state in a material causes yielding. Note, the von Misescriterian is based on the strain energy density associated with a change in shape at a material point.

The von mises stress is defined as the uniaxial tensile stress that would create the same distortion energy as is created by the actual combination of the applied stress.

For ductile materials, the von mises effective stress is calculated by either directly from the applied stress or from the principle stress those results from those applied stress note that the effective stresses calculation convertsany combination of 2D or 3D Applied stresses at a point into a single stress value.

That can be compared with suitable strength criterion.

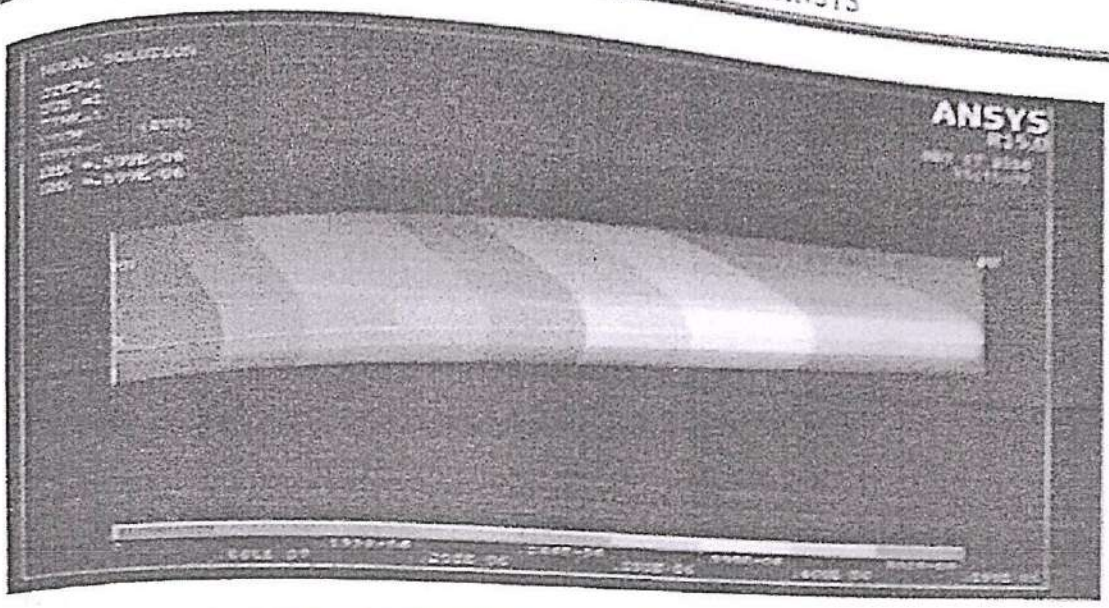


Fig.6.2USUM for loading 2 under max pressure 56KN/m^2

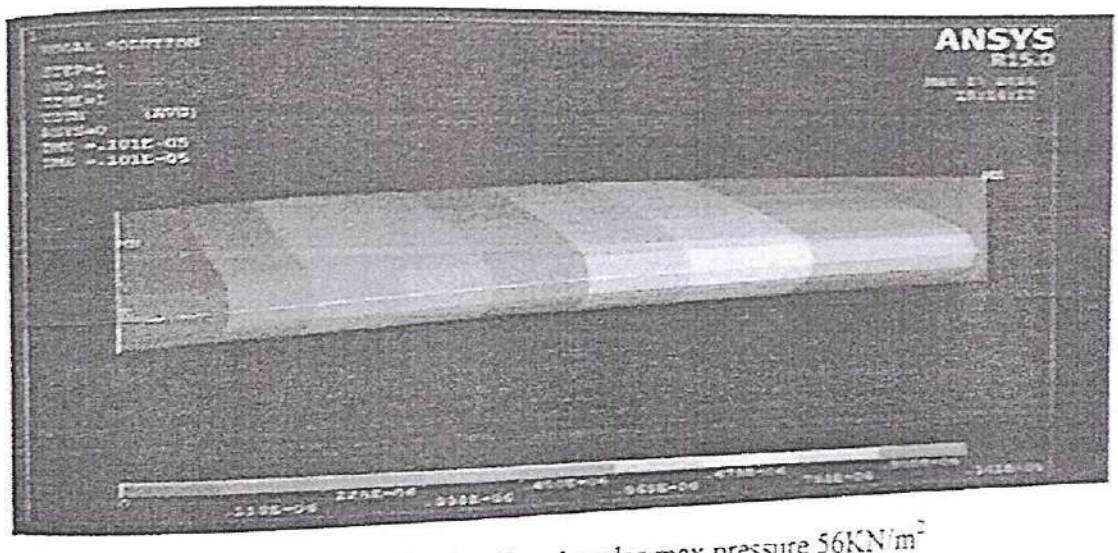


Fig.6.3USUM for loading 4 under max pressure 56KN/m^2

Fig.6.4USUM for loading 6 under max pressure 56KN/m^2

CONCLUSION:

From the above results we can conclude that the difference between the values of deformation, equivalent stress, max principle stress, stress intensity and shear stress of AA 2024 T351 are minimal. The results obtained are validated and verified.

- In this project, an aircraft wing is modeled in modeling software AUTODESK INVENTOR and the airfoil chosen is NACA-4412 and 2410.
- Analysis is done on Aircrafts wing using ANSYS software by applying air pressure to AA 2024 T351 material. By observing the analysis results, the deformation and stresses are less for wing. Maximum stress is identified at wing root which is found out to be lower than yield strength of the material. Normally the fatigue crack initiates in a structure where there is maximum tensile stress is located.
- We can perform the parametric analysis with the use of different parameters like Material properties, loadingcondition, boundary condition, mesh resizing by virtue of which we obtain some useful information without experimental cost.
- Comparing the waveforms S-N graphs of the high cycle fatigue researchof 2024 alloy material it can be concluded that the longitudinal samples (to sheet rolling direction) exhibit significantly better fatigue life than the transverse samples.
- This project helped in understanding various software's and analyzing it under various conditions and different stresses.
- Through the project the applications of the tools present in the software has become easy and all the complex parts are being made appropriately with ease.
- The use of FE Software ANSYS and its components allow faster and efficient model generation. Almost all structurally important components could be modeled using ANSYS Preprocessor. The application of varied types of loads and boundary condition is also simple.

PRINCIPAL
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

Head of Department
Mechanical Engineering
Navodaya Institute of Technology (NIT)
RAICHUR-584 103

NAVODAYA INSTITUTE OF TECHNOLOGY RAICHUR